University of Glamorgan

Faculty of Advanced Technology

Design and Verification of SC-FDE/OFDM Communication Schemes for Millimetre-Wave Wireless System Using FPGA Technologies

PhD 2012

Khaled Sobaihi

A thesis submitted in partial fulfilment of the requirements for the degree of Doctor of Philosophy

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Director of Studies: Dr. Akram Hammoudeh

Second Supervisor: Dr. David Scammell

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I declare that the thesis has not been, nor currently being, submitted for award of any other degree or similar qualification

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All the praises and thanks be to God, Lord of the universes.

Abbreviations and Acronyms

ADC	analog-to-digital converter
AGC	automatic gain controller
APSK	amplitude and phase shift keying
ASK	amplitude shift keying
AWGN	additive white Gaussian noise
BER	bit error rate
BPSK	binary phase shift keying
CP	cyclic prefix
CE	channel estimation
CMOS	complementary metal-oxide-semiconductor
CFR	channel frequency response
DAC	digital-to-analog converter
DBPSK	differential binary phase shift keying
DFE	decision feedback equalization
DFT	discrete Fourier transformation
DPD	digital predistortion
DPSK	differential binary phase shift keying
DQPSK	differential quadrature phase shift keying
DR	dynamic range
DSP	digital signal processing
ECMA	European Computer Manufacture Association
EHF	extremely high frequency
EIRP	equivalent isotropically radiated power
FB	feedback
FCC	Federal Communications Commission
FD-DFE	frequency domain decision feedback equalization
FDE	frequency domain equalization
FDM	frequency-division multiplexing
FEC	forward error correction
FFT	fast Fourier transform
FM	frequency modulation
FSK	frequency shift keying
GSM	global system for mobile communications
HDR	high data rate
HDTV	high-definition television
ICI	inter-carrier interference
IDFT	inverse discrete Fourier transform
IF	intermediate frequency
IFFT	inverse fast Fourier transform or inverse fast Fourier transformation
ISI	inter-symbol interference
ISM	industrial, scientific and medical
LAN	local area network
LNA	low noise amplifier
LO	local oscillator
LOS	line-of-sight
LSB	least significant bit

LTE	long-term evaluation
LUT	look-up table
MAC	media access control
MAM	M-ary amplitude modulation
MC	multiple-carrier
MIMO	multiple-input-multiple-output
MSB	most significant bit
MMSE	minimum mean squared error
MSE	mean squared error
NLOS	non-LOS
OBO	output back-off
OFDM	orthogonal frequency-division multiplexing
OOK	on/off keying
PA	power amplifier
PAPR	peak-to-average power ratio
PER	packet error rate
PHY	physical layer
PLL	phase-locked loop
PN	pseudo noise
PSK	phase shift keying
QAM	quadrature amplitude modulation
QPSK	quadrature phase shift keying
RF	radio frequency
RMS	root mean square
RRC	root raised cosine
Rx	receiver
SC	single-carrier
SC-FDE	single-carrier with frequency domain equalizer
SDR	software defined radio
SFD	start of frame delimiter
SISO	single-input-single-output
SNR	signal-to-noise ratio
TDD	time division duplex
Tx	transmitter
UW	unique word
UWB	ultra wideband
UW-SC	unique word single carrier
VCO	voltage controlled oscillator
VNA	Vector Network Analyser
Wireless HD	Wireless high definition
WLAN	wireless local area networks
WPAN	wireless personal area network

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Abstract

This thesis contributes to the development and characterization of millimetre-wave personal area networks (WPANs) in the 60 GHz frequency band. Single-carrier and multicarrier transmission techniques are considered in the implementation of a 64.8 GHz WPAN capable of achieving a reliable indoor link. Thus, single-carrier with frequency domain equalization (SC-FDE) and orthogonal frequency-division multiplexing (OFDM) communication schemes were designed and implemented to mitigate the multipath fading of the 60 GHz indoor channels. As a result, a complete millimetre-wave transceiver operating at 64.8 GHz, with up to 100 Mb/s data-rate utilizing 16-QAM modulation scheme is realized.

The re-programmability offered by field-programmable gate arrays (FPGAs) along with their capability of performing real-time digital signal processing has been exploited. A FPGA-based platform is employed to prototype the hardware implementation of the baseband digital signal processing modules of the proposed 64.8 GHz millimetre-wave transceiver. The design and the construction of the complete baseband transceiver is based on a software-defined radio (SDR) concept, which was achieved by a software and hardware implementation of different functional modules of the digital baseband transceiver.

The baseband transceiver has been successfully interfaced with a 64.8 GHz radio system which was built using commercially available discrete RF modules. The back-to-back performance of both baseband transceiver and the 64.8 GHz WPAN has been validated.

The performance of the implemented transceiver has been characterized in different transmission scenarios, within different environments, and with line-of-sight and non-line-of-sight conditions. This characterization has been performed by measuring the bit-error rate (BER) against signal-to-noise ratio (SNR) in different communication scenarios.

The work presented in this thesis shows that a 64.8 GHz WPAN can be successfully implemented with either SC-FDE or OFDM communication scheme. Also, the advantage of SC-FDE and its ability to be a prominent alternative to the OFDM in multipath channels is presented.

The novel aspects of this thesis are summarized as follows:

1. Design, implementation, and performance verification of a 64.8 GHz WPAN using SC-FDE and OFDM communication schemes together with frequency domain equalization (FDE).

2. BER characterization and performance evaluation in indoor multipath channels for various use cases scenarios.

CHAPTER I
General Introduction

I.1 Introduction

Currently wireless services are being deployed for personal, home, local, metropolitan, and wide-area networks from a small to a larger geographical area. The wireless wide-area networks (WWANs) provide wireless access to regional-wide and city-wide areas. The wireless metropolitan area networks (WMANs) allow communication between two or more terminals in the range of about 5 km; the most well-known WMAN is the WiMax (Worldwide Interoperability for Microwave Access). The wireless local-area networks (WLANs) are commonly used to provide a wireless access through an access point to the internet. This gives users the mobility to move within a local area such as a building. The IEEE 802.11 standard known as the Wi-Fi is the most known WLAN. The wireless personal-area network (WPAN) is a network for interconnecting electronic devices wirelessly; this usually takes place in the surrounding of an individual's workspace within about 10 metres diameter circle. Typical operational ranges and data-rates for these wireless networks are illustrated in Figure I-1.

The existing WPAN technologies such as ZigBee and Bluetooth are essentially designed for low-power and low data-rate applications, such as interconnecting between computers and their peripherals devices, connecting sensors to actuators, or connecting devices in cars without the need of cables. The frequency band employed in these technologies is the license free industrial, scientific and medical (ISM) radio band. The ISM frequency bands are relatively crowded and not suitable for high-data, particularly for video applications, where a large bandwidth is required to support high data-rate, as high as multi-gigabit-per-second (Multi-Gb/s). The ultra-wideband (UWB) technology, which operates in the 3.1 to 10.6 GHz frequency range, presents one possible solution to achieve such high data-rate. However, the UWB is highly restricted in term of allowable transmit power levels imposed by regulatory bodies [1].

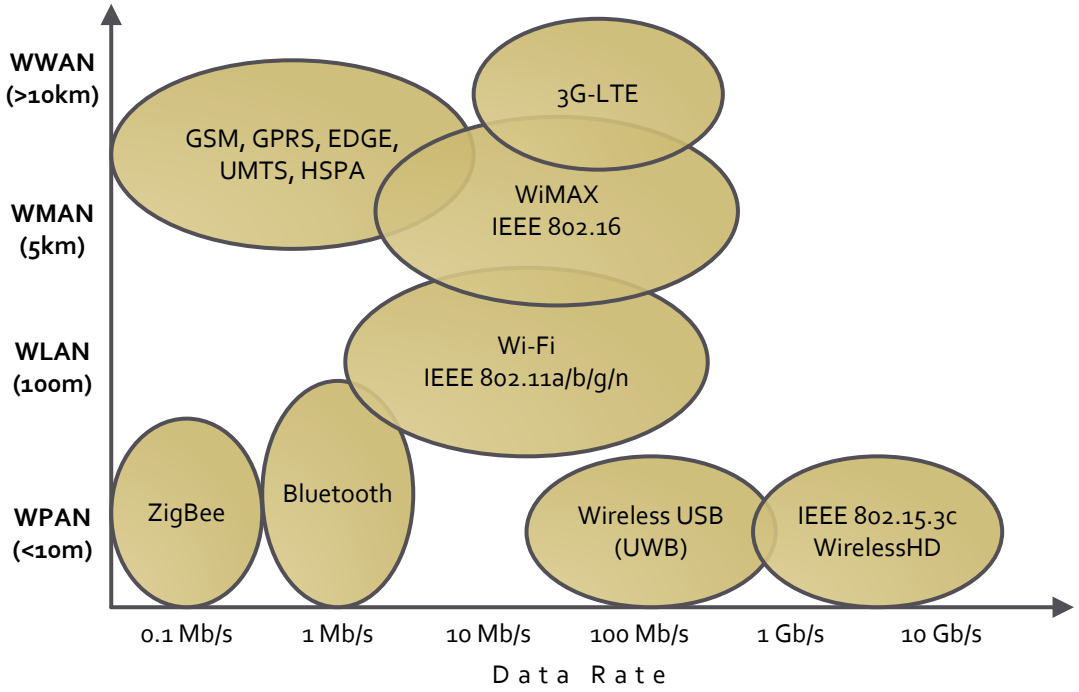


Figure I-1 Operational Range and Data-Rate for WWAN, WMAN, WLAN, and WPAN Networks

The large bandwidth around the 60 GHz is one of the largest unlicensed bandwidths ever allocated. The allocated frequency band is up to 7 GHz, with a common bandwidth of around 3.5 GHz, provides a great potential for gigabit-per-second (Gb/s) wireless applications. In addition, compared to the unlicensed bandwidth allocated for UWB, the 60 GHz bandwidth is continuous and less restricted in terms of power limits.

Furthermore, the tiny and compact size of the 60 GHz antennas allow smart-antenna solution to be easily implemented in mobile and handheld devices which is difficult if not impossible at lower frequencies. As a result, and with the recent advances in silicon process technologies and low-cost integration solutions, the 60 GHz technology has attracted a great deal of interest from academia, industry and standardization bodies.

I.2 The 60 GHz Industrial Standardization

The standardization of the 60 GHz unlicensed frequency band is currently being developed by several industrial consortia and standardization bodies to realize multi-Gb/s wireless transmission.

In March 2004, the IEEE 802.15.3c Task Group (TG3c) was created to develop a new millimetre-wave based physical layer (PHY) for the existing IEEE 802.15.3b WPAN standard. The developed PHY targets a minimum data-rate of 2 Gb/s over a few metres with optional data rates that are up to 5 Gb/s. In September 2009, the IEEE-SA standards board has approved the IEEE 802.15.3c-2009 to be the final release of this standard [2]. This was the first standard for multi-gigabit data-rates solution for many applications, especially those related to wireless multimedia applications, such as high speed internet, HDTV video streaming, and wireless data bus for cable replacement.

In 2007, the "WirelessHD" has also released a specification to enables consumer devices to create a wireless video area network (WVAN), which uses the unlicensed 60 GHz band to send uncompressed HD video with a typical range of at least 10 metres for the highest resolution HD Video. The "WirelessHD" group believes that 60 GHz will allow a theoretical data rates of up to 20 Gb/s, permitting stream of uncompressed video and audio up to quad full HD (QFHD) resolution, with 48 bit colour and 240 Hz refresh rates [3].

Also in 2009, the wireless gigabit alliance (WiGig) was working together with the IEEE 802.11ad Task Group (TGad) to define the physical (PHY) and medium access control (MAC) layers that are based on IEEE 802.11ac standard, to enables native support for IP networking over 60 GHz. The WiGig specification targets data transmission rates up to 7 Gb/s with beamforming, enabling robust communication at distances beyond 10 metres [4].

I.3 IEEE 802.15.3c for 60 GHz WPAN

The IEEE 802.15.3c is the first standard that addresses multi-gigabit data rate for short-range wireless system. This standard supports up to 2 Gb/s over few metres with an optional data rate up to 5 Gb/s. Released in Sep. 2009, the IEEE 802.15.3c defines three operating modes for different applications, and a common mode allowing different PHY layers to communicate [2]:

Single-Carrier (SC PHY) Mode: this mode targets low-power and low-cost applications using single carrier block transmission (SCBT). The SC PHY supports operation in non-line-of-sight as well as line-of-sight, with or without equalization.

Three data-rate's classes are defined, 1st class for kiosk file downloading with data-rates up to 1.5 Gb/s, the 2nd class targets desktop/office devices connectivity and achieves up to 3 Gb/s, and Class 3 support high-performance applications with data-rates exceeding 3 Gb/s.

High Speed Interface (HSI PHY): the HSI mode is designed for bidirectional high-speed data-rates using omnidirectional antennas and orthogonal frequency-division multiplexing (OFDM). This mode mainly targets computer's peripherals connectivity (e.g., printers, data storages, etc.) that requires low-latency.

Audio/Visual (AV PHY): This mode is designed for multimedia applications and has two PHY, high-rate PHY (HRP) and low-rate (LRP). Both use the OFDM to transmit uncompressed HD video streaming.

Table I.1 summaries the three PHY modes specifications defined by the IEEE 802.15.3c standard. The common mode signalling (CMS) is low rate transmission (25 Mb/s) with single-carrier PHY mode that enables inter-operability among different PHY modes, and beamforming [5].

Table I.1 PHY Modes of the IEEE 802.15.3c Standard

Feature	SC-FDE	HSI OFDM	AV OFDM
Modulation	BPSK, QPSK, 8-PSK, 16-QAM	QPSK, 16-QAM, 64-QAM	QPSK, 16-QAM
Coding	Reed Solomon/LDPC	LDPC	Convolutional/ Reed Solomon
Data Rate	25.8 - 5280 Mb/s	32.1 - 5005 Mb/s	952-1904 Mb/s
Training Sequences	Golay Code	Golay Code	PN/Barker-13 Sequences
Occupied Bandwidth	1782 MHz	1782 MHz	1760 MHz

I.4 Usage Models of the IEEE 802.15.3c

The IEEE 802.15.3c targets five possible consumer's applications, presented in Figure I-2, these include files transfers, audio-visual broadcasting, and networking [6]:

Uncompressed HD Video Streaming UM1/UM2: Due to the large available bandwidth in the 60 GHz band, uncompressed HDTV can be transmitted wirelessly from high-definition video player, HD Camera recorder, or gaming console to single or multiple display devices. The IEEE 802.15.3c assumes 1920×1080 pixel resolution, 24 bit/pixel video signal, and a rate of 60 frames/s. The required data rate is over 3.5 Gb/s, and the maximum distance is around 5 metres for non-line-of-sight and 10

metres for line-of-sight. These usage models are defined by UM1 and UM2 for single and multiple displays respectively.

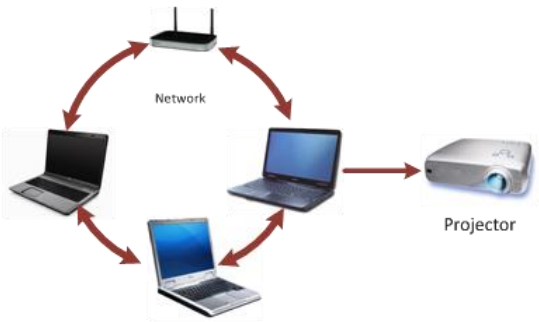
Office/Desktop Connectivity (UM3): This UM defines unidirectional/bidirectional connections between personal computer PC and different peripherals, including printers, displays, and hard disk. The environment could be a furnished desktop or office with line-of-sight or non-line-of-sight view. Retransmission is allowed and maximum distance is around 5 metres.

Conference ad hoc (UM4): In this scenario many computers are communicating with each other using one 802.15.3c network. The maximum data rate is 1.75 Gb/s with distances between 1 and 5 metres should be achieved with a maximum bit-error rate of 10^{-6}.

Kiosk File-Downloading (UM5): This is an electronic kiosk providing a video and music files download and upload from a near distance with users hold handheld devices (e.g., Smartphone, Camera). Data-rates of 1.5 and 2.25 Gb/s are required at 1 metre distance.

Single/Multiple HDTV Video Streaming UM1/UM2

PC-Peripherals Connectivity UM3



Conference ad hoc UM4

Kiosk File-downloading UM5

Figure I-2 Usage Models Targeted by the 802.15.3c Standard

I.5 Aims and Objectives

The primary aim of this thesis is to design, implement, validate, and characterize a millimetre-wave wireless communication system transceiver. Single-carrier with frequency domain equalization (SC-FDE) and orthogonal frequency-division multiplexing (OFDM) communication schemes are considered in the implementation of the baseband modulation schemes of this wireless system.

Employing the software-defined radio (SDR) concept, a field-programmable gate array (FPGA) is adopted as digital signal processing platform, for the software and hardware implementation of all the baseband signal processing functions required in such radio system. The baseband transceiver design is based on the IEEE 802.15.3c PHY standard. The 16-QAM modulation scheme with frequency domain equalization technique is adopted to achieve 100 Mb/s data-rate.

To realize the millimetre-wave wireless communication link, a 64.8 GHz wireless transmitter/receiver terminals are employed as RF frontends for the implemented baseband transceiver. The back-to-back performance of both baseband and millimetre-wave transceiver have been validated.

The completed 64.8 GHz millimetre-wave wireless communication system is then employed to enable the characterization of the bit-error rate (BER) performance of both SC-FDE and OFDM communication schemes. Measurements of bit-error rate (BER) against signal-to-noise ratio (SNR) are performed in a number of indoor channels, with different transmission scenarios and with line-of-sight (LOS) and non-line-of-sight (NLOS) conditions.

Those results will provide an understanding of the capabilities and limitations of the SC-FDE and OFDM communication strategies, over the 60 GHz millimetre-wave frequency band.

I.6 Thesis Outline

The thesis is organized as follows:

Chapter II: this chapter analysis the characteristics, and features of the 60 GHz frequency band. The indoor radio channels model and RF frontend employed in the 60 GHz frequency band are introduced along with the potential baseband modulation schemes adopted in the 60 GHz and their advantages and disadvantages.

Chapter III: this chapter introduces the concept of software-defined radio (SDR). It includes definitions, and functional architecture of SDR. Moreover, this chapter discusses the trade-offs of different digital signal processing platform choices to implement the SDR.

Chapter IV: details the FPGA-based design and implementation of the single-carrier with frequency domain equalization (SC-FDE) and orthogonal frequency-division multiplexing (OFDM) baseband transceivers. Analysis and tests of the baseband transceiver are performed for preliminary performance evaluation, together with the resource requirement.

Chapter V: this chapter describes the interfacing of the baseband transceiver to the 64.8 GHz radio system to facilitate the 64.8 GHz wireless mobile radio link. It also presents the measurement geometry of the indoor channels employed together with the experimental setups employed for LOS and NLOS measurement scenarios. The back-to-back verification of the hardware and system performance validation is also described.

Chapter VI: this chapter presents results of the experiments made using the hardware of Chapter V in number of indoor environments under LOS and NLOS conditions. Results given for different use case scenarios are presented as bit-error rate (BER) versus signal-to-noise ratio (SNR). Capabilities and limitations of SC-FDE and OFDM techniques are characterized in different scenarios and communication constraints.

Chapter VII: this provides general conclusions that summarize the results obtained from this study in the context of the aims and objectives. It also provides pointers to future studies.

CHAPTER II
The 60 GHz Wireless Personal Area Network (WPAN)

II.1 Introduction

The worldwide availability of the huge amount of contiguous, and unlicensed spectral space in the 60 GHz band provides wide room for gigabit-per-second (Gb/s) wireless applications. Recently, the 60 GHz frequency band has attracted interest from academia, industry, and global standardization bodies to develop multi-Gb/s applications such as high definition multimedia interface (HDMI) cable replacement for uncompressed video streaming, gigabit Ethernet, and multi-Gb/s file transfer.

II.2 Worldwide Frequency Allocation

Certainly, one of the major advantages of the 60 GHz technology over the existing wireless systems is the huge, contiguous unlicensed bandwidth offered, which presents a great potential to achieve gigabit-per-second data-rate in wireless applications.

Figure II-1 shows the 60 GHz frequency spans that have been allocated for different countries and regions. In Europe, the European conference of postal and telecommunications administrations (CEPT) released in October 2009 the latest deployment of the 60 GHz, 9 GHz (57-66 GHz) of unlicensed bandwidth is allocated for outdoor application having a maximum power of 25 dBm with power density of -2 dBm/MHz and for indoor applications a maximum power of 40 dBm with a maximum spectral power density of 13 dBm/MHz is specified [5].

In North America, the federal communications commission (FCC) allocates 7 GHz in the 57-66 GHz band for unlicensed uses allows an average power density of 9 $\mu W/cm^2$ at 3 metres and a maximum power density of 18 $\mu W/cm^2$ at 3 metres. These values translate to average and maximum equivalent isotropically radiated power (EIRP) of 40 dBm and 43 dBm respectively, taking RF safety issues into account, the FCC recommends a maximum transmit power that is limited to 10 dBm. In 2000, the ministry of public management, home affairs, posts and telecommunications (MPHPT) of Japan issued 60 GHz radio regulations for unlicensed utilization in the

59–66 GHz band with maximum transmit power limited to 10 dBm and maximum allowable antenna gain of 47 dBi [5, 7]. Table II.1 illustrates the 60 GHz unlicensed frequency band, maximum transmit power, EIRP and maximum antenna gain in different countries and regions.

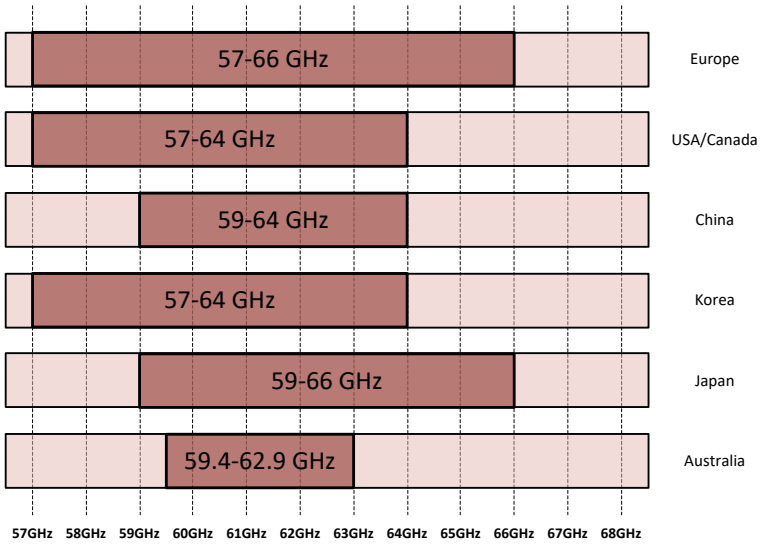


Figure II-1Worldwide Frequency Allocation for 60 GHz Band

Table II.1 Frequency Bands, Maximum Transmit Power, EIRP, and Antenna Gain for Different Regions

Region	Unlicensed Bandwidth (GHz)	Maximum Transmit Power	EIRP (dBm)	Maximum Antenna Gain (dBi)
Europe	9	20mW/13 dBm	57.0 dBm	30.0 dBi
USA/Canada	7	500mW/27 dBm	40-43 dBm	33 dBi with Transmit = 10 dBm
Japan	7	10mW/10 dBm	58.0 dBm	47.0 dBi
Korea	7	10mW/10 dBm	27.0 dBm	17.0 dBi
Australia	3.5	10mW/10 dBm	51.7 dBm	41.8 dBi

II.3 60 GHz Channel Characterization and Modelling

Knowing the propagation characteristics of the millimetre-wave 60 GHz radio channels is the fundamental issue for designing wireless transceiver systems. A radio channel model can provide detailed insight into the complex radio wave propagation mechanisms and allows study of the achievable performance from both theoretical and simulation standpoints [5].

Figure II-2 shows the propagation paths that links two wireless devices in an indoor radio channel. The direct path known as line-of-sight is the shortest path and undergoes a free space propagation, the non-line-of-sight propagation paths are the

result of different reflexions off the walls, ceiling, and objects and reach the receiver with different delays, this is knows as multipath fading and induces random fluctuations in the received signal level.

In a typical radio channel, on a very short distance scale in the order of a wavelength, the fluctuations in the received signal power are called small-scale fading. The received signal strength fluctuates over the distance of a number of wavelengths as well, and referred as large-scale fading. The large scale fading is due to either path loss or shadowing in the propagation channel. Two types of small-scale fading exist [8]:

Time-selective fading: time selectivity of the channel is caused by the Doppler effect in the mobile channel, where transmitter/receiver terminals or objects within the channel are in motion. Therefore, time-selective fading occurs due to the time-variant environments of the wireless channel. Depending on how rapidly the channel changes relative to data-rate, the channels are classified either as a fast fading channel or slow fading channel.

Frequency-selective fading: this is due to the time dispersion of the transmitted signal within the channel, the channel is classified either as flat fading or frequency selective fading. In the flat fading the spectral characteristics of the transmitted signal are preserved at the receiver, whereas, in frequency selective channel, certain frequency components of the received signal spectrum have greater gains than others.

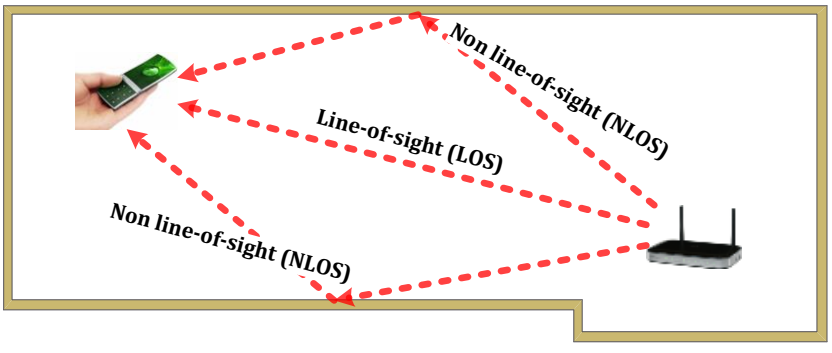


Figure II-2 Line-of-sight and Non-line-of-sight Propagation in Multipath Radio Channel

II.3.1 Free Space Propagation

Like any electromagnetic wave propagation, the path loss in free space of the millimetre-wave depends on the wave length λ and distance R, as follows:

$$L_{free\ space} = 20\log_{10}\left(4\pi\frac{R}{\lambda}\right)\ \text{dB} \qquad \text{Eq. II.1}$$

This equation describes a line-of-sight (LOS) propagation in free-space, where the loss increases with frequency and distance. Considering all the factors from the transmitter to the receiver, the received power P_{Rx} is a function of the transmitted power P_{Tx}, and the gain of the transmit antenna G_{Tx} and receive antenna G_{Rx} with respect to isotropic radiator, the free space path loss is given by Friis equation in dBm:

$$P_{Rx} = P_{Tx} + G_{Tx} + G_{Rx} + 20\log_{10}\left(\frac{\lambda}{4\pi R}\right)\ \text{dBm} \qquad \text{Eq. II.2}$$

In addition to the free space loss, there are also absorption loss factors, such as oxygen and water vapour absorption in the transmission medium. The millimetre-wave around 60 GHz is highly absorbed by the oxygen and the factors that affect millimetre-wave propagation are given in Figure II-3. In addition, depends on the rain intensity rain adds further losses of a few dB. This poses a severe challenges to deliver a reliable 60 GHz outdoor link, these make the 60 GHz mainly reserved for backhaul applications with highly directional antenna that point to each other in a line-of-sight scenario [5].

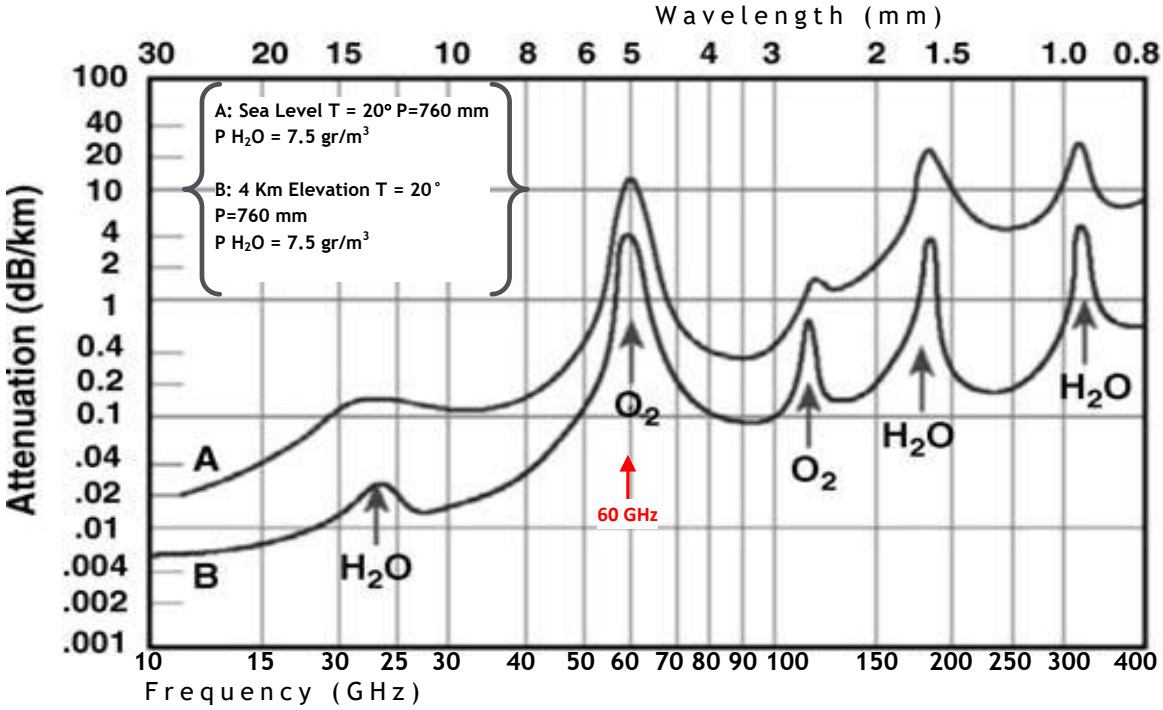


Figure II-3 Atmospheric Absorption of Millimetre-Waves Propagation

II.3.2 IEEE 802.15.3c Industry Standard Channel Model

IEEE 802.15.3c channel models are mainly derived based on wideband measurement results conducted in typical office, residential, library and desktop environments. For each environment, line-of-sight and non-line-of-sight scenarios were considered [9].

Figure II-4 shows the geometry description of a typical furnished office environment, the measurement system is based in the frequency sweep technique that requires a vector network analyser (VNA) to measure the frequency response of the radio channel.

Table II.2 and Table II.3 give the specifications of the propagation measurement system and description of different modelled channels respectively [10].

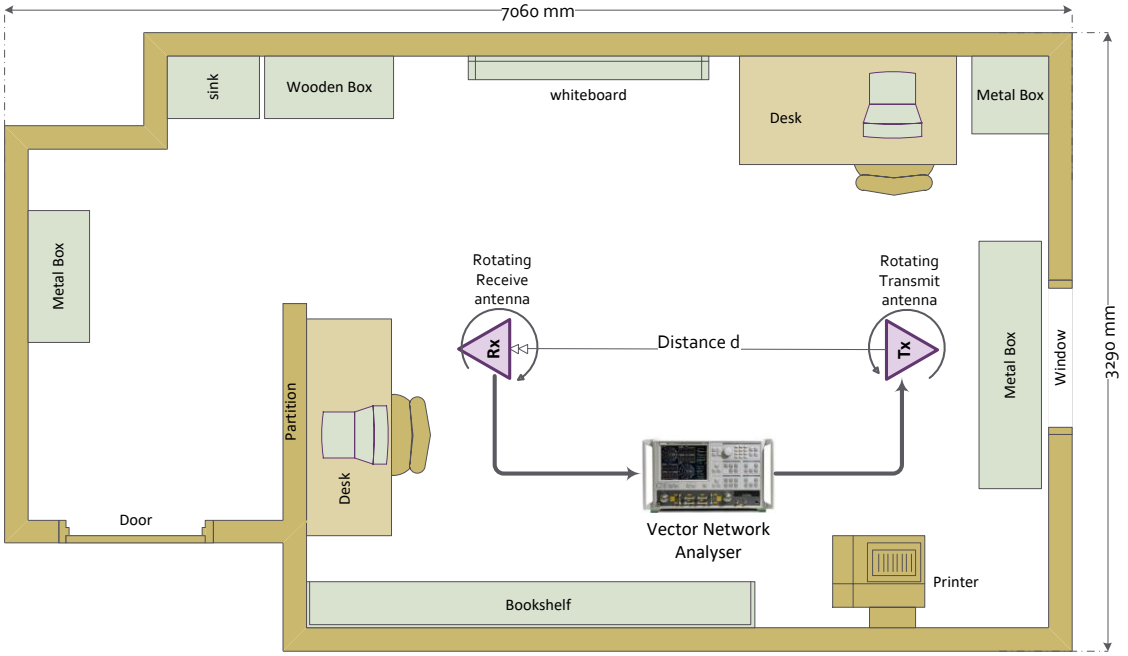


Figure II-4 Wideband Propagation Measurements in Typical Office Environment

Table II.2 Details of Propagation Measurements

VNA Instrument	HP8510CVNA
Centre frequency	62.5 GHz
Bandwidth	3 GHz
Tx and Rx antennas	Conical horn antenna (16 dBi) Beamwidth are 30°
Rotational step angle	5°
Distance between Tx and Rx	d=1,2,3 metres

Table II.3 Description of Different Environments Modelled by the IEEE 802.15.3c [10]

Channel Model	Scenario	Environment	Descriptions
CM1	LOS	Residential	Typical home with multiple rooms and furnished with furniture, TV sets lounges, etc. The size is comparable to the small office room. The walls/floor is made of concrete or wood covered by wallpaper/carpet. There are also windows and wooden door in different rooms within the residential environment.
CM2	NLOS		
CM3	LOS	Office	Typical office setup furnished with multiple chairs, desks, computers and work stations. Bookshelves, cupboards and whiteboards are also interspersed within the environment. The walls are made by metal or concrete covered by plasterboard or carpet with windows and door on at least one side of the office. Cubical, laboratory, open and closed office can be treated as a generic office. Typically these offices are linked by long corridors.
CM4	NLOS		
CM5	LOS	Library	Typical small size library with multiple desks, chairs and metal bookshelves. Bookshelves are filled with books, magazines, etc. Some tables and chairs were interspersed between the bookshelves. At least one side of room has windows and/or door. The walls are made of concrete.
CM6	NLOS		
CM7	LOS	Desktop	Typical office desktop and computer clutter. Partitioning surrounded this environment.
CM8	NLOS		
CM9	LOS	Kiosk	Typical kiosk server with human body holding a portable device, The portable device is pointed to the kiosk server.

II.3.2.1 Large-Scale Characterization

Unlike the narrowband, the wideband and ultra-wideband systems, such as the 60 GHz, the path loss (PL) is both distance and frequency dependent. The IEEE 802.15.3c models the average path loss as follows [5]:

$$\overline{PL}_{(d)} = \underbrace{PL_{d_0}[dB]}_{\substack{path\ loss\ at\ reference \\ distance\ d_0}} + \underbrace{10n\log_{10}\left(\frac{d}{d_0}\right)}_{\substack{path\ loss\ exponent\ at \\ distance\ d}} + \underbrace{\sum_{q=1}^{Q} X_q}_{\substack{attenuation\ due \\ to\ obstruction}} + \underbrace{X_\sigma[dB]}_{\substack{Shadowing \\ Fading}} \qquad \text{Eq. II.3}$$

The IEEE 802.15.3c defines the path loss (PL) for residential and office in both line-of-sight and non-line-of-sight. Table II.4 shows the parameters of the PL models, these parameters were derived based on measurements using different setups and propagation scenarios, with reference distance d_0=1 metre, and transmit G_{Tx} and

receive G_{Rx} antenna gains equal to zero dBi. The term X_q accounts for the additional attenuation due to specific line-of-sight obstruction by objects.

The factor σ_s describes the shadowing effect, where due to the dynamic evolution of propagation paths, the average signal power received over a large area (a few tens of wavelengths) varies around an average value, measurement results reported in the 60 GHz range have shown that the shadowing fading is log-normally distributed, $X_\sigma[dB] = N(0, \sigma_S)$, where X_σ denotes a zero-mean Gaussian random variable measured in decibels with standard deviation σ_S. The value of σ_S is listed in Table II.4 for different environments.

Table II.4 Path Loss at d_0, and Exponent *n* defined by the IEEE 802.15.3c [9]

Environment	Scenario	n	PL_0	σ_s	Transmit/Receive antenna Beamwidth
CM1	LOS	1.53	75.1	1.5	TX 72°, RX 60°
CM2	NLOS	2.44	86.0	6.2	TX 72°, RX 60°
CM3	LOS	1.16	84.6	5.4	TX Omni, RX horn 30°
CM4	NLOS	3.74	56.1	8.6	TX Omni, RX horn 30°

II.3.2.2 Small-Scale Characterization

When compared with other narrowband indoor wireless systems (e.g., 2.4 and 5 GHz), which consist of vector summation of many irresolvable paths as a result of limited capability of the system measurement bandwidth, the amplitude fading distributions are typically Rayleigh and Rician for NLOS and LOS scenarios, respectively. Whereas, for the 60 GHz indoor wideband systems, the small-scale fading can follow a variety of distributions depending on type of environment, measurement bandwidth and scenarios [5].

The IEEE 802.15.3c has adopted the generic complex impulse response (CIR) that takes into account the clustering phenomenon. The cluster model is based on the extension of the Saleh–Valenzuela (SV) model to the angular domain [11].

In addition, measurement results show that when directive antennas are used, especially in the LOS scenario, there appeared a distinct strong LOS path on top of the clustering phenomenal [9]. Figure II-5 shows the complex impulse response (CIR) as a function of time of arrival (ToA), and angle of arrival (AoA). Hence, the complex

impulse response $h_{(t,\ \emptyset,\ \theta)}$ which gives the amplitude of the ray that arrives at time t, with angle of arrival ϕ and angle of departure θ by:

$$h_{(t,\ \emptyset,\ \theta)} = \underbrace{\beta\delta(\tau,\phi,\theta)}_{LOS} + \sum_{l=0}^{L}\sum_{k=0}^{K_l} \underbrace{a_{k,l}\delta\big(t - T_l - \tau_{k,l}\big)\delta\big(\emptyset - \Omega_l - \omega_{k,l}\big)\delta\big(\theta - \Psi_l - \psi_{k,l}\big)}_{Clusters} \qquad \text{Eq. II.4}$$

Where:

$\delta(.)$: Dirac delta function,

$\beta\delta(\tau,\phi,\theta)$: is the gain of the straight LOS path,

L, K_l : the number of clusters and number of rays in the K^{th} cluster respectively,

$a_{k,l}$, $\tau_{k,l}$, $\omega_{k,l}$, and $\psi_{k,l}$: Complex amplitude, time of arrival (ToA), angle of arrival (AoA) and angle of departure (AoD) of the k^{th} ray of the l^{th} cluster,

T_l, Ω_l, Ψ_l : The mean ToA, mean AoA, and mean AoD of the l^{th} cluster.

The angle of arrival of each ray within a cluster $\omega_{k,l}$ can be modelled either by zero-mean Gaussian or zero-mean Laplacian distribution with standard deviation $\sigma_{\emptyset}$. Whereas, the angle of arrival mean Ω_l of each cluster is uniform distributed over [0, 2π][5].

The average number of clusters $\bar{L}$ is typically from 3 to 14. Since the clustering phenomenon is due the effect of superstructure (e.g., walls, furniture, computers and doors), higher number of clusters would be expected in cases where the environment under consideration has more furnishing [9].

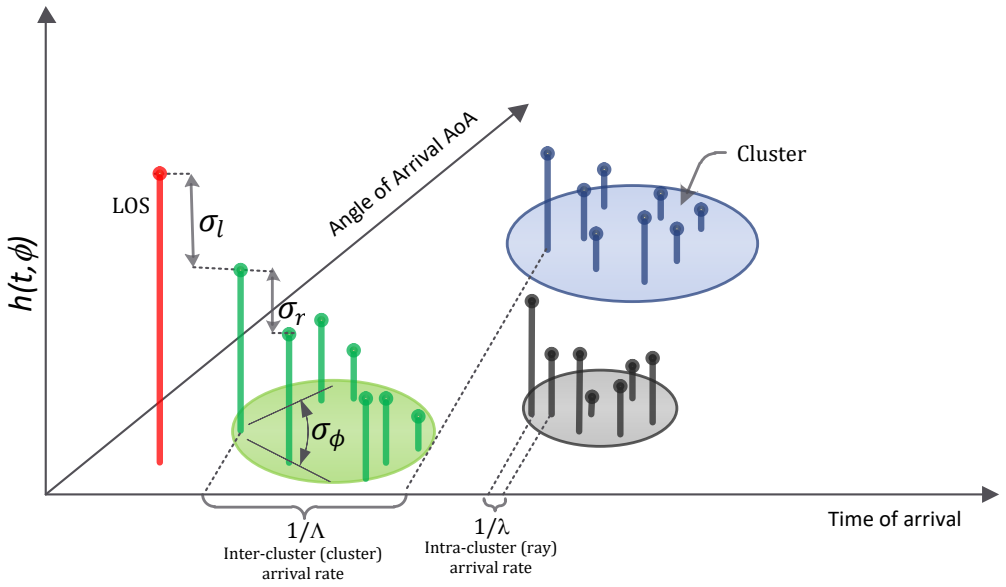


Figure II-5 Channel Impulse Response as a Function of ToA and AoA

II.3.2.3 Power Delay Profile

The power delay profile of a channel is the received average power as a function of an excess delay with respect to the first arrival path, Figure II-6 illustrates a power delay profile (PDP) as function of time of arrival of each ray within each cluster, the cluster arrival $1/\Lambda$ and the ray arrival $1/\lambda$ times are described by two independent Poison processes:

$$p(T_l|T_{l-1}) = \Lambda\left[-\Lambda e^{(T_l - T_{l-1})}\right] \quad l > 0 \qquad \text{Eq. II.5}$$

$$p\left(\tau_{k,l}\middle|\tau_{(k-1),l}\right) = \lambda\left[-\lambda e^{\left(\tau_{k,l} - \tau_{(k-1),l}\right)}\right] \quad k > 0 \qquad \text{Eq. II.6}$$

Where Λ and λ are the cluster arrival rate and ray arrival rate, respectively. The mean amplitude of the clusters and the amplitude of each ray within a cluster are modelled with log-normal distribution. Due to the propagation delays and internal successive reflections within clusters, clusters and rays exponentially decay by the order of $e^{-t/\Gamma}$ and e^{-t/γ_r} respectively [12].

Table II.5 shows the channel parameters for LOS residential environment CM1.1 with T_x = 360°, R_x = 15°, parameters of other environments are given in reference [5].

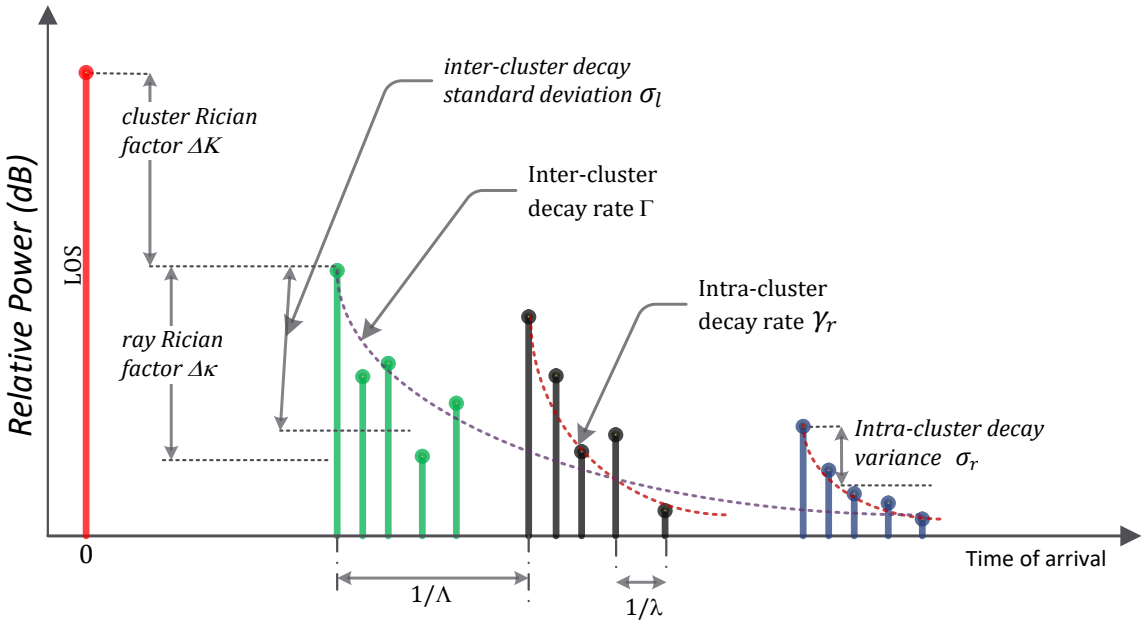


Figure II-6 Power Delay Profile as Function of Time of Arrival

Table II.5 Parameters for LOS residential environment CM1.1

Parameters	description	LOS CM1.1 Tx = 360°, Rx = 15°
Λ [1/ns]	inter-cluster arrival rate	0.191
λ [1/ns]	intra-cluster (ray) arrival rate	1.22
Γ	clusters' amplitude decay rate	4.46
$\boldsymbol{\gamma_r}$	intra-cluster (ray) amplitude decay rate	6.25
σ_c [dB]	cluster log-normal standard deviation	6.28
σ_r [dB]	rays log-normal standard deviation	13.00
σ_ϕ [degrees]	AoA Laplacian standard deviation	49.8
$\bar{\boldsymbol{L}}$	average number of clusters	9
Δk [dB]	ray Rician factor	18.8
Ω(d) [dB]	average power of the first ray in the first cluster	–88.7 dB (d = 3 metres)
n_d	path loss exponent	2

A Matlab code is provided by the IEEE 802.15.3c channel modelling group to generate complex impulse response (CIR) and power delay profile (PDP) of the considered channels. Figure II-7 illustrates an example of a power delay profile (PDP) of CM1.1 channel.

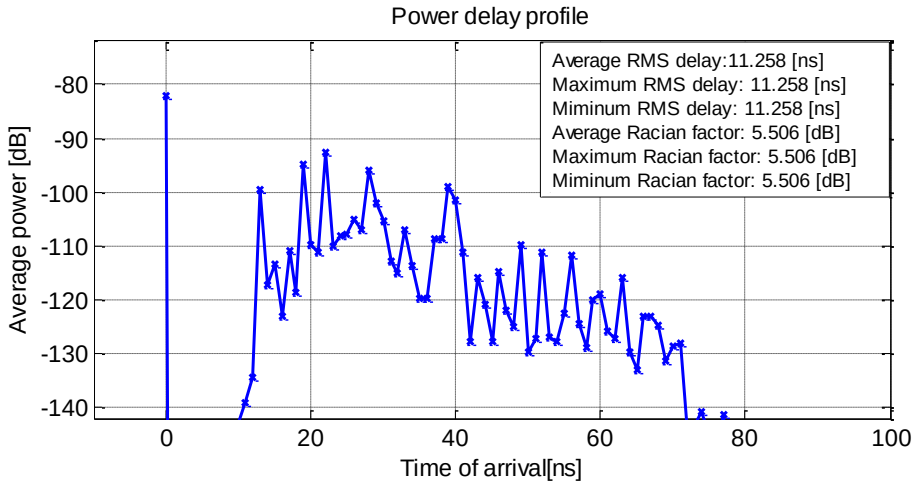


Figure II-7 Power delay profile (PDP) example of CM1.1 channel

In order to quantify the multipath channel, a number of important dispersion parameters can be derived from the PDP. Those are: the mean excess delay, root mean squared (rms) delay spread, and excess delay spread.

The most considered parameter in wireless system design is the rms delay spread, which is a second moment of the PDP that statistically measures the time dispersion of a channel. The rms delay spread (τ_c) is inversely proportional to the coherence bandwidth B_c of a channel, which determines the maximum achievable data rate without inter-symbol-interference (ISI). The rms delay spread is given by [8]:

$$\sigma_\tau = \sqrt{\overline{\tau^2} - (\bar{\tau})^2} \qquad \text{Eq. II.7}$$

$$\text{Where } \bar{\tau} = \frac{\sum_k P(\tau_k)\tau_k}{\sum_k P(\tau_k)} \text{ and } \overline{\tau^2} = \frac{\sum_k P(\tau_k)\tau_k^2}{\sum_k P(\tau_k)} \qquad \text{Eq. II.8}$$

II.4 Digital Modulations for 60 GHz

The choice of the digital modulation for 60 GHz depends on several factors, such as spectrum efficiency, linearity of power amplifier, channel's characteristics, targeted applications etc. There are two major categories of digital modulations that have been adopted in the 60 GHz communications. The first category is binary modulation where single bit is transmitted at a time; the second category is M-ary modulations, called multi-levels modulations where it is possible to transmit more than two bits at a time. Single-carrier and multicarrier transmission techniques are adopted to implement the M-ary modulations for 60 GHz.

II.4.1 Binary Modulations

II.4.1.1 On/Off Keying

The on/off keying (OOK) modulation is the simplest modulation that can be employed; it consists only of turning on and off the carrier signal with a binary unipolar signal. Hence, the waveform of the OOK modulated carrier of amplitude A_c and frequency f_c can be written as:

$$x_{(t)} = \begin{cases} A_c \sin 2\pi f_c t & \text{for digital 1} \\ 0 & \text{for digital 0} \end{cases} \qquad \text{Eq. II.9}$$

The OOK modulator can be practically implemented as an analogue multiplier (i.e., Mixer) used to multiply the binary data (formatted as unipolar signal) with a carrier sine wave as shown in Figure II-8.b. This has the advantage of switching off the transmitter when transmitting '0', which conserves power [7, 13].

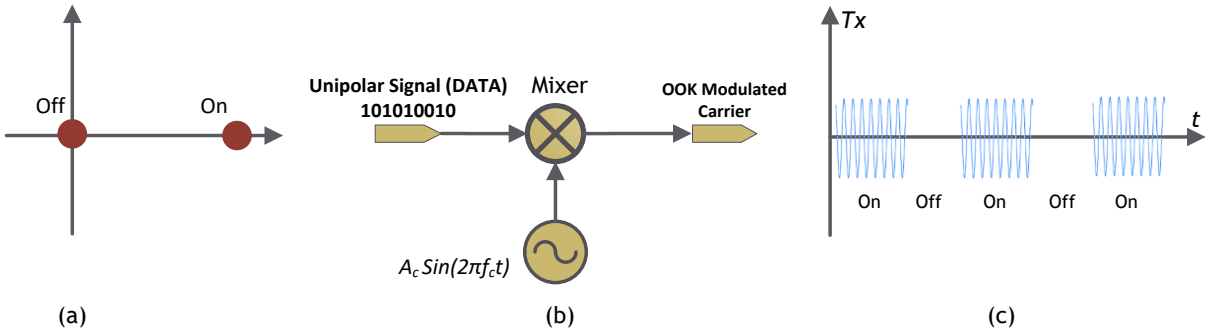


Figure II-8. OOK Modulation Diagram (a), its System Diagram (b), and the OOK Waveform (c)

As shown in Figure II-9.a, coherent demodulation where the carrier frequency has to be regenerated at the receiver to recover the original OOK signal, and non-coherent demodulation, Figure II-9.b, could be employed for demodulation, where after band-pass filtering an envelope detector eliminates the carrier and keeps only the OOK signal.

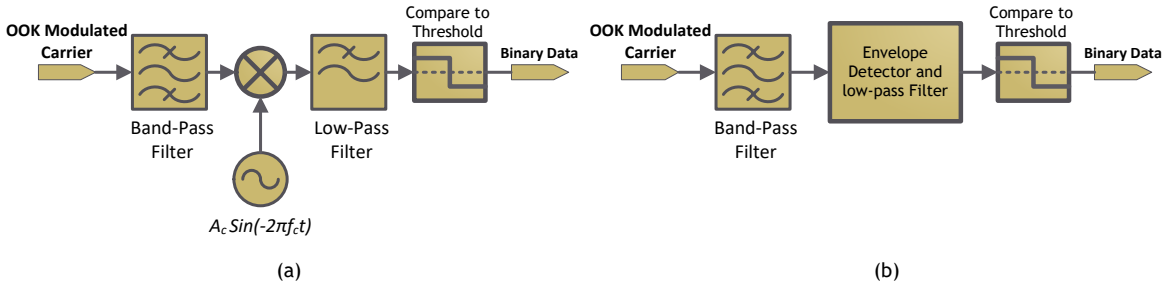


Figure II-9. Coherent (a) and Non-Coherent (b)Demodulation for OOK

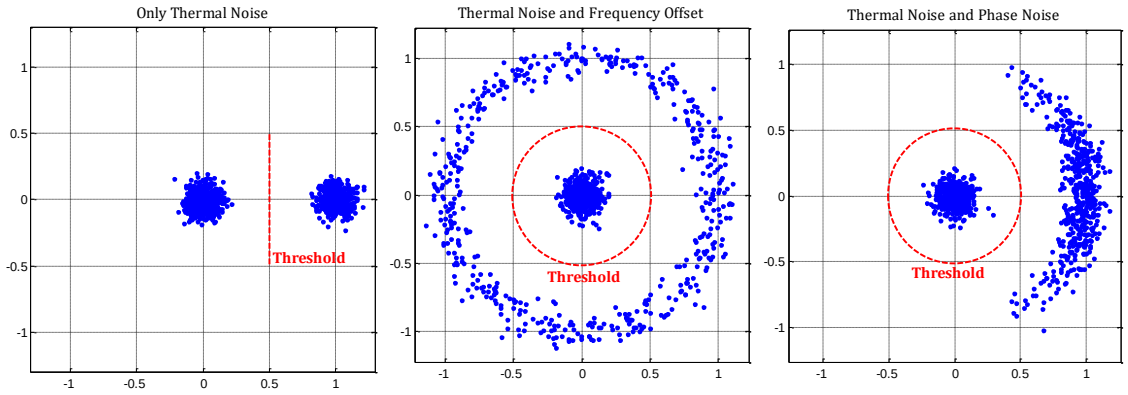


Figure II-10. Thermal Noise, Frequency Offset, and Phase Noise Effect on OOK Modulation

As shown in Figure II-10, either in the presence of thermal noise, carrier offset, or phase noise, a threshold is fixed to be equal to half the amplitude of the carrier for a minimum probability of error, in this case probability of error P_e is as follows [7]:

$$P_e = \frac{1}{2}\text{erfc}\left(\frac{A_c}{2\sqrt{2}\sigma_n}\right) \qquad \text{Eq. II.10}$$

Where σ_n is the noise power and erfc() the complementary error function defined as:

$$\text{erfc}(z) = \frac{2}{\sqrt{\pi}}\int_z^{\infty} e^{-t^2}\,dt \qquad \text{Eq. II.11}$$

II.4.1.2 Frequency Shift Keying (FSK)

Frequency shift keying (FSK) is a special type of the analogue frequency modulation (FM) in which the message signal is a baseband digital signal. In this modulation, bits 1 and 0 are represented by a pair of orthogonal signals as follows [14]:

$$S_{MSK}(t) = \begin{cases} A\cos(2\pi f_1 t + \theta_1), & for\ \ bit = 1 \\ A\cos(2\pi f_2 t + \theta_1), & for\ \ bit = 0 \end{cases} \qquad \text{Eq. II.12}$$

With:

$$f_1 = f_c - \frac{1}{2T_b}, \quad \text{and } f_2 = f_c + \frac{1}{2T_b}$$

Where and in order to preserve the orthogonality of the two frequency f_1 and f_2, the carrier f_c is a multiple of the bit-rate $\frac{1}{T_b}$, with $f_c = l\frac{1}{T_b}$, where $l > 1$.

II.4.1.3 Minimum Shift Keying (MSK)

The MSK was derived from FSK modulation with continuous-phase modulation which make the peak-to-average power ratio equals to zero dB, this feature has made this modulation an attractive option for the 60 GHz system, where the nonlinearity problem of the power amplifiers in the transmitter is more serious [5].

MSK can be seen as a form of FSK modulation, MSK signal is given by:

$$S_{MSK}(t) = \begin{cases} \sqrt{\frac{2E_b}{T_b}}\cos\left(2\pi f_1 t + \theta_{(0)}\right), & for\ \ bit = 1 \\ \sqrt{\frac{2E_b}{T_b}}\cos\left(2\pi f_2 t + \theta_{(0)}\right), & for\ \ bit = 0 \end{cases} \qquad \text{Eq. II.13}$$

Where E_b is the transmitted signal energy per bit, and $\theta_{(0)}$ the initial phase, the two frequencies f_1 and f_2 satisfy:

$$f_1 = f_c - \frac{1}{4T_b}, \quad \text{and } f_2 = f_c + \frac{1}{4T_b}$$

In MSK, the spacing between f_1 and f_2 is the minimum that allows the detection of the received signal at the receiver; this explains the name minimum shift keying. To produce smooth transition from one binary state to another of the MSK signal, the baseband signal is sinusoidally filtered as shown in Figure II-11.

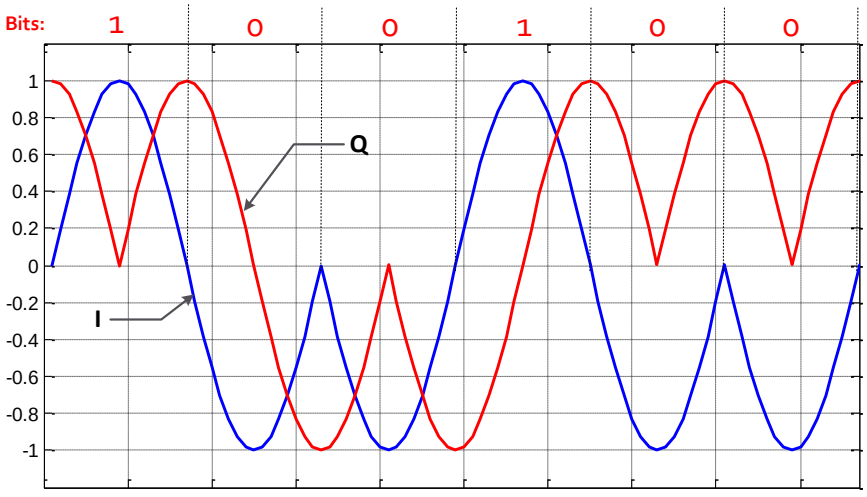


Figure II-11 Real (I) and Imaginary (Q) Components of MSK Signal

II.4.1.4 Gaussian Minimum Shift Keying (GMSK)

The GMSK is a special case of MSK modulation, where the uses of a pre-modulation low-pass filter with Gaussian characteristics reduces considerably the transmitted bandwidth of the signal and suppress out-of-band noise. Thus, GMSK provides high spectrum efficiency, excellent power efficiency and a constant amplitude envelope that allows class C power amplifiers to be employed to minimize power consumption. Figure II-12 shows the spectra of different modulation schemes, those spectra show the advantage of GMSK compared to MSK where fast spectral roll-off is achieved with GMSK modulation, resulting high attenuation of out-of-band frequencies and noise. Furthermore, the GMSK has even faster spectra roll-off than QPSK filtered with square-root raised cosine filter, and zero peak-to-average power ratio (PAPR).

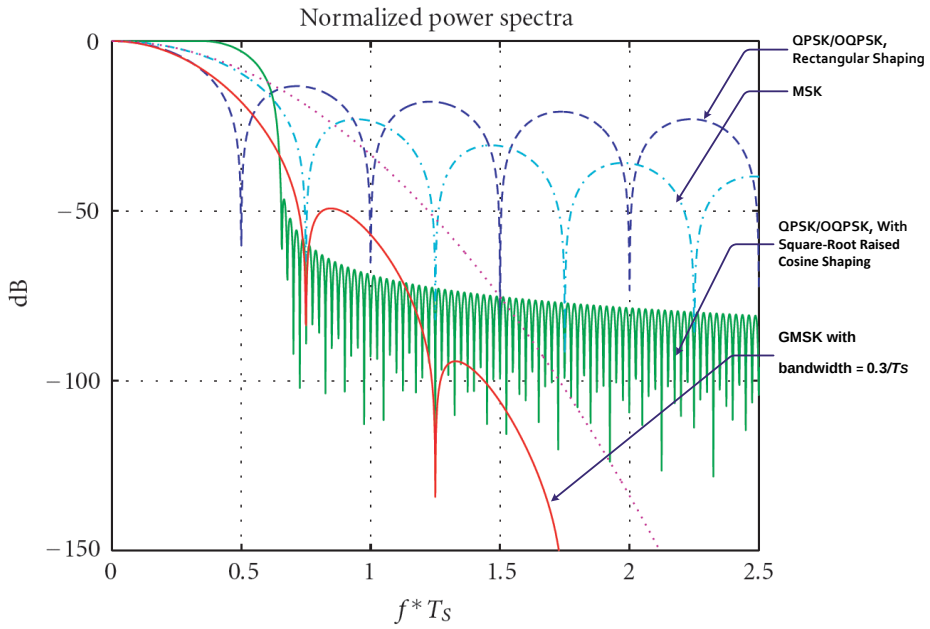


Figure II-12 Spectra of Different QPSK, MSK and GMSK Modulations [15]

The previous binary modulations have the drawback of low spectral efficiency, where the highest spectral efficiency is achieved with GMSK modulation whit 1.35 bits/s/Hz. The bit energy-to-noise ratio E_b/N_0, in an AWGN channel is around 8–14 dB for binary modulation. Whereas, the Shannon limit shows that a much higher spectral efficiency (6 bits/s/Hz) can be achieved in this range of E_b/N_0 [14]. To achieve higher spectral efficiency, M-ary modulations such as 16-QAM, 256-QAM etc. come into the

picture. Those modulation can be implemented either in single-carrier (e.g., SC-FDE) or multicarrier (e.g., OFDM) modulation scheme.

II.4.2 Orthogonal Frequency-Division Multiplexing (OFDM)

Orthogonal frequency-division multiplexing (OFDM) is a modulation scheme that is widely used in high data-rate wireless communication systems, because of its robustness against frequency selective fading. In OFDM, the high data-rate stream is converted to a parallel low-rate sub-streams, each low-rate sub-stream occupies only a narrow frequency band [13]. The OFDM can be seen as a multiplexing technique, where the transmitted signal is the linear sum of multiple carriers (called subcarriers), each of those subcarriers are modulated independently with different modulation schemes (e.g., BPSK, QPSK, 16-QAM, etc.).

II.4.2.1 OFDM Principle

Making X_n the modulated data symbols to be transmitted over the n^{th} subcarrier, f_n the frequency of the n^{th} subcarriers, the OFDM waveform which is the summation of N subcarriers in time domain is written as:

$$x_{(t)} = \sum_{n=0}^{N-1} X_n \, e^{j2\pi f_n t} \qquad \text{Eq. II.14}$$

In discrete time, with T_s the sampling time and m the samples' index, the waveform of Eq. II.14 becomes:

$$x_{(kT_s)} = \sum_{n=0}^{N-1} X_n \, e^{j2\pi f_n k T_s} \qquad \text{Eq. II.15}$$

Furthermore, suppose that the N subcarriers are equally spaced in the frequency domain with a minimum frequency separation equal to $\frac{1}{NT_s}$, the OFDM signal is given by:

$$x_{(kT_s)} = \sum_{n=0}^{N-1} X_n \, e^{j2\pi kn/N} \qquad \text{Eq. II.16}$$

As long the minimum separation is respected, the $k_1{}^{th}$ and the $k_2{}^{th}$ subcarriers with $k_1 \neq k_2$ are orthogonal, this can be expressed as:

$$\sum_{n=0}^{N-1}(e^{\frac{j2\pi k1}{N}n}) \times (e^{\frac{j2\pi k2}{N}n})^* = \sum_{n=0}^{N-1} e^{\frac{j2\pi(k1-k2)}{N}n} = \delta_{k1,k2} \qquad \text{Eq. II.17}$$

Where (.)* denotes the complex conjugate, and $\delta_{k1,k2}$ is the Kronecker delta function. Figure II-13 illustrates the frequency and time domain of the orthogonal subcarriers.

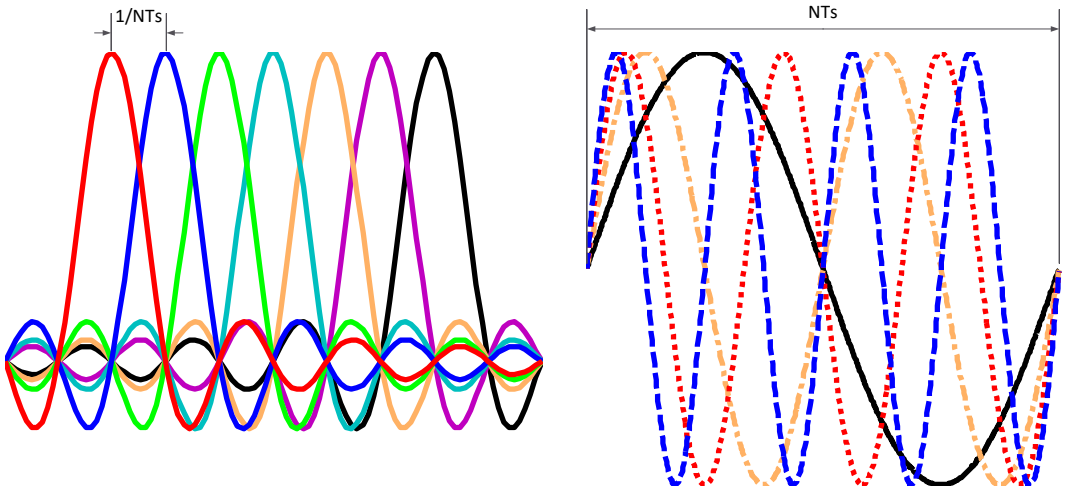


Figure II-13. Frequency Domain (a) and Time Domain (b) of the OFDM Subcarriers

When examining the OFDM signal of Eq. II.16, it can be shown that this signal can be obtained simply by applying a discrete inverse Fourier transform (IDFT) of N data symbols; this can be implemented in an efficient way by using inverse fast Fourier transform (IFFT). Figure II-14 illustrates an OFDM transmitter/receiver, where after data is modulated to symbols, N-points IFFT is applied then serialized prior to transmission. At the receiver, and after that the received samples is parallelized back, N-Points FFT is performed to recover the origin modulated symbols; those symbols are then demodulated to extract data.

When the OFDM signal is transmitted over frequency selective multipath channel, interference of the OFDM inter-symbol interference (ISI) and inter-carrier interference (ICI) may occur. To mitigate these interferences, a cyclic prefix (CP) is inserted at the transmitter by copying the last M symbols of the OFDM block to the beginning and then removed at the receiver, as long the length of the cyclic prefix is greater than the channel delay spread, inter-symbols interference is avoided as shown in Figure II-15.

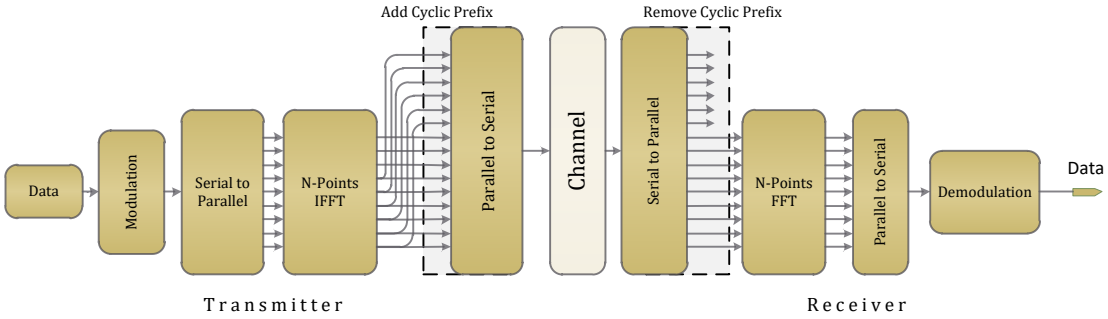


Figure II-14. FFT-Based OFDM Transmitter/Receiver

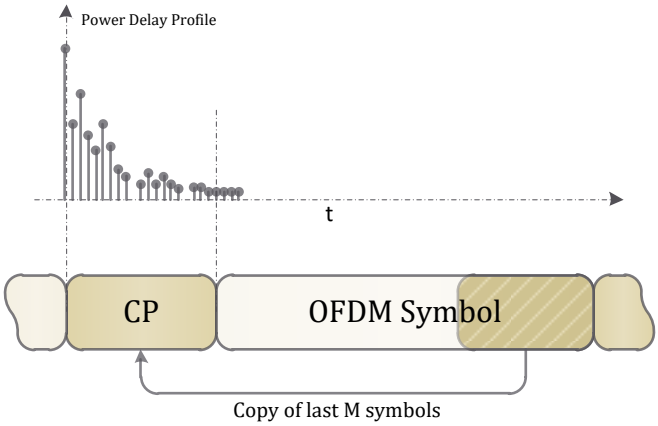


Figure II-15. Cyclic Prefix Insertion

II.4.2.2 Advantages and Drawbacks of OFDM

The advantages and drawbacks of an OFDM system can be summarized as follows [16]:

Advantages:

❖ High spectral efficiency due to the overlapped and nearly rectangular frequency spectrum of the subcarriers,

❖ Robustness against channel's frequency selectivity since it effect only a couple of subcarriers, coding and interleaving among subcarriers can mitigate this effect,

❖ Reduced computational complexity by employing FFT transform,

❖ Flexible spectrum shaping can be realized by annulling some subcarriers.

Drawbacks:

❖ As any multicarrier signal, OFDM signal has very high peak-to-average power ratio (PAPR), this will influence the linearity of the power amplifier and signal

clipping may happen. Hence, OFDM requires RF power amplifiers with high peak to average power ratio,

- High sensitivity to carrier frequency offset and phase noise (due to local oscillators jitters) than single-carrier system,
- Loss in spectral efficiency due the cyclic prefix insertion.

II.4.3 Single-Carrier with Frequency Domain Equalization (SC-FDE)

One of the major drawbacks of the OFDM relative to single-carrier is the very high peak-to-average power ratio (PAPR) of the transmitted signal; this makes the OFDM signal vulnerable to nonlinearity of the transmitter power amplifier. However, when SC modulations are employed in a high data-rate transmission over a severe time-dispersive channel, the signal bandwidth exceeds the coherence bandwidth of the radio channel, leading to severe signal distortion unless a complex receiver with equalization is employed. However, the complexity of time-domain equalizers increase linearly with the length of the channel impulse response, with the impulse response of a 60 GHz indoor channel spreads over hundreds of samples, this leads to very high computational complexity at the receiver [17].

The SC-FDE is a combination of OFDM and SC, where high PAPR of the OFDM is avoided, with frequency-domain equalization that was mainly reserved for OFDM. This can be achieved if symbols are mapped into blocks and separated by a cyclic prefix.

Figure II-16 shows the conversion between OFDM to SC-FDE. In OFDM system the IFFT transform is placed at the transmitter to map the data symbols into subcarriers. In SC-FDE the IFFT is placed at the receiver to transform the equalized spectrum to time domain for demodulation [18].

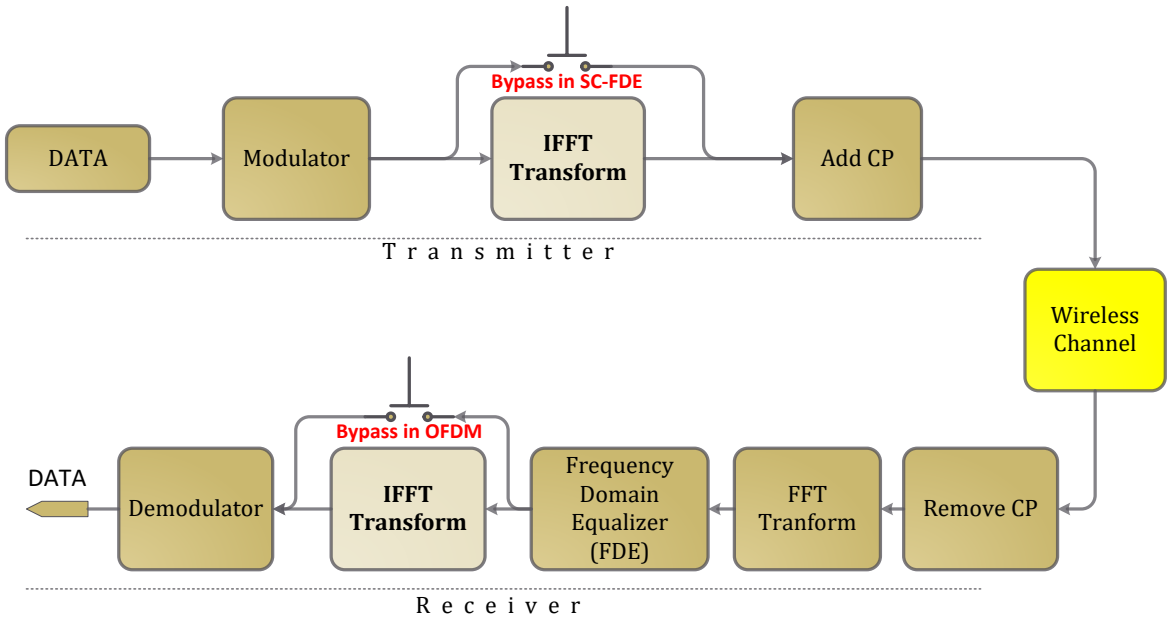


Figure II-16 Duality between FFT-Based SC-FDE and OFDM

II.4.3.1 Frame Structure of SC-FDE

Figure II-17 shows a general frame structure employed in SC-FDE, a burst frame consists of a preamble, a header, and a payload packet. The preamble consists of a synchronization (SYNC) sequence to help the receiver's algorithms related to automatic gain control and timing/carrier frequency recovery. The start frame delimiter (SFD) is used to mark the beginning of the header and payload frames. The channel estimation sequence (CES) field are used to perform time-domain channel estimation prior to FDE equalization [7].

As shown in Figure II-17, and in order to apply frequency domain equalization on a single-carrier transmission, data symbols are gathered into blocks, where the FFT transform is applied at the receiver. Therefore, similar to an OFDM system, guard interval (GI) is appended at the beginning of each block in order to mitigate inter-block interference in a dispersive channel.

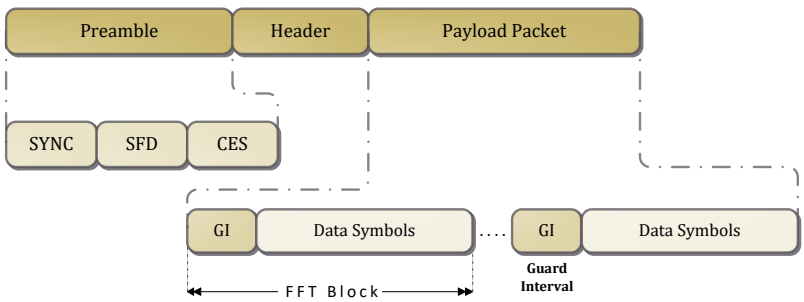


Figure II-17 Frame Structure for SC-FDE Wireless Systems

II.5 RF Frontend Architectures for 60 GHz

Two transceiver architectures can be employed to transmit and receive complex modulation, super-heterodyne architecture where the up/down conversion is performed in at least two steps, and direct-conversion architecture where the up/down conversion is done in one step [19].

II.5.1 Super-Heterodyne Architecture

This architecture has been the standard implementation for wireless receivers due to its high selectivity and sensitivity. The super-heterodyne transceiver shown in Figure II-18 uses two frequency conversion stages, each stage includes one local oscillator (LO), a mixer and filtering. At the receiver, a band-pass filter rejects all out-of-band signals among the RF signals collected by the antenna, The in-band signal is then amplified by a low-noise amplifier (LNA) to keep noise floor as low as possible. The first RF LO is tuned at the RF frequency to convert the channel of interest into an intermediate frequency (IF). A band-pass filter (BPF) then suppresses the generated image of this conversion before a second IF LO is mixed with the IF signal to be down converted to IQ baseband signals. A low-pass filter (LPF) is then applied on the IQ baseband signal to remove any out-of-band frequencies. An automatic gain control (AGC) is employed before IQ mixer to adjust signal levels for optimum IQ demodulation operation [19].

In the real world, as shown in Figure II-19, combinations of frequency-division and multiplication are employed in a super-heterodyne architecture to generate the RF and IF LOs. A division factor of two is employed since it is one of the best-known ways of obtaining quadrature signals. The frequency multipliers that are based on the inherent nonlinear property of semiconductor devices, by which it is possible to implement frequency multiplication factors of 2, 3, 4 or more at millimetre-wave frequencies in both SiGe and CMOS are used to generate high frequency RF LOs [5].

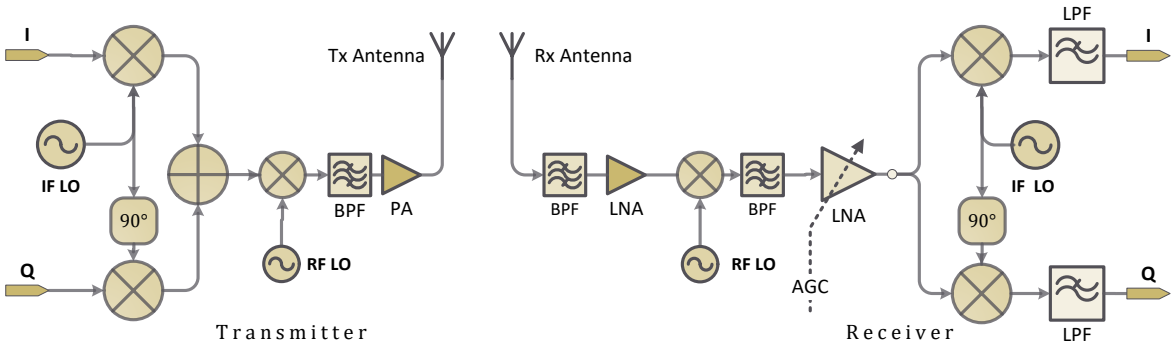


Figure II-18 Super-Heterodyne RF Frontends Architecture

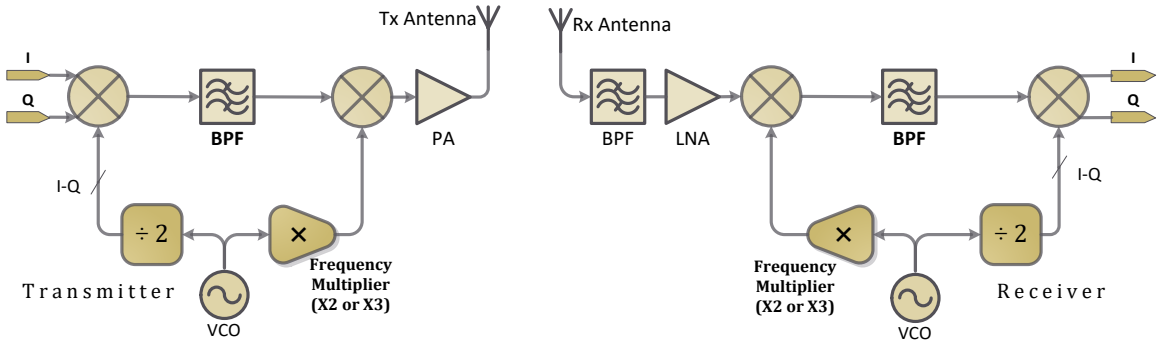


Figure II-19 Super-Heterodyne Transceiver Architecture Using Frequency Multiplier

II.5.2 Direct-Conversion Architecture

Direct-conversion architecture, also known as zero-IF or homodyne architecture is the simplest solution for low-cost and low-power 60 GHz transceiver. Hence, the direct-conversion implementation is usually employed in handset devices. In comparison with super-heterodyne architecture, direct-conversion translates RF directly to baseband signal in one step. Therefore, direct-conversion does not require any image rejection filters; this makes it suitable for monolithic one-chip integration.

The basic architecture of direct conversion is illustrated in Figure II-20, one power amplifier (PA) and one low-noise amplifier (LNA) is employed in the transmitter and the receiver respectively [1]. This architecture is based on the IQ mixers principle to modulate/demodulate both amplitude and phase of the carrier. Therefore, a local oscillator with in-phase and quadrature (90° shift) outputs are required, mixed with the baseband in-phase (I) and quadrature (Q) components to up-convert the baseband signal to RF frequency. The inverse process is performed in the receiver, where the RF signal mixed with local oscillator with a frequency equals to that used in the transmitter, is translated to complex IQ baseband signal.

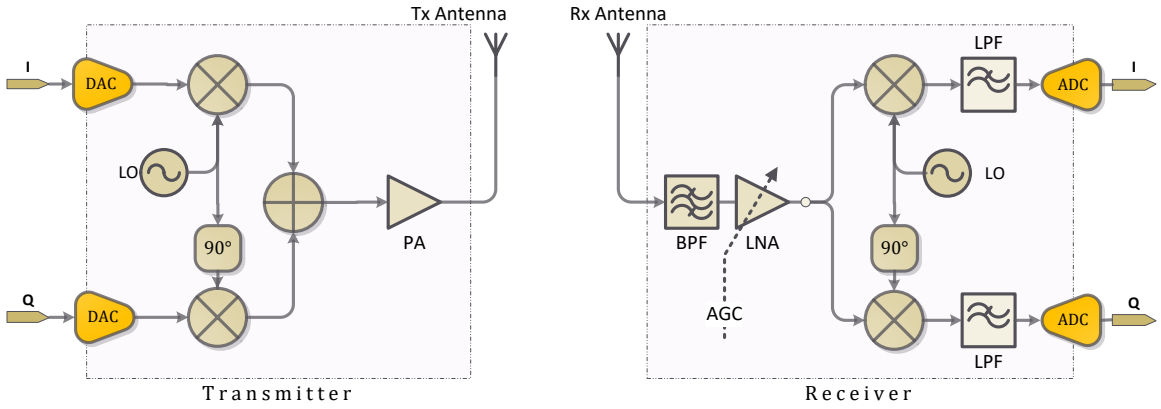


Figure II-20 Architecture of Direct Conversion Transceiver

II.6 RF Impairments in 60 GHz Frontend

For low-cost implementation of radio systems operating at 60 GHz frequency band, most components used in the transmission chain work under non-ideal conditions or work ideally only in a limited range. These imperfections tend to corrupt the signals and degrade the transmission performance.

II.6.1 Nonlinear Power Amplifier

Due to high nonlinearity characteristics of semiconductor devices around the millimetre-wave frequency band, the silicon-based 60 GHz power amplifiers exhibit severe distortion. Due to this, the transmitter is unable to radiate enough power while keeping high linearity.

Figure II-21 shows the output power as function of input power of a typical 60 GHz power amplifier fabricated by the SiGe process. This shows that beyond certain input power, the output power stops increasing linearly and the gain start to drop with degradation of the power efficiency. To quantify the power efficiency, power added efficiency (PAE) as function of input power is considered, the PAE, denoted by η is defined as the ratio of amplified output power to DC power that supplies the amplifier:

$$\eta = \frac{P_{out} - P_{in}}{P_{dc}} \qquad \text{Eq. II.18}$$

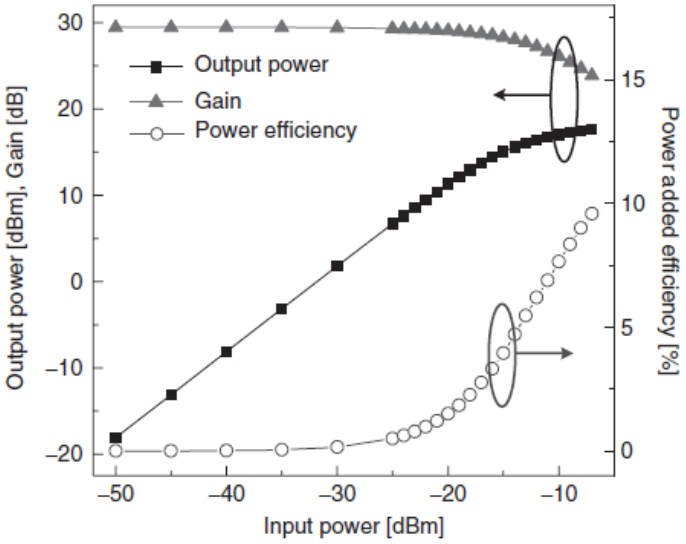


Figure II-21 Output Power, Gain and Power Efficiency Vs. Input Power of a Power Amplifier[5]

For the sake of modelling the power amplifier, a behavioural model that characterizes the power amplifier's nonlinearity is considered. Assuming the power amplifier is time-invariant, based on third-order polynomials the output $y_{(t)}$as a function of input signal $x_{(t)}$ is as follows:

$$y_{(t)} = a_1 x_{(t)} + a_2 x_{(t)}^2 + a_3 x_{(t)}^3 \qquad \text{Eq. II.19}$$

Where a_1 is small signal linear gain, and a_2 and a_3 are nonlinear coefficients attributed to first and second harmonics respectively.

Figure II-22 shows the output power versus input power, suppose the input signal is a single-tone, $x_{(t)} = A\sin(\omega t)$, the compression point is defined as the input power level where the gain drops by 1 dB (IP1dB), this corresponds to the output power (OP1dB). Slightly above this point the output power ceases to increase and the amplifier becomes saturated. However, decreasing the output power, the PA can deliver a larger linear region at the expense of less efficiency. Thus, an optimal operating point where the PA meets the required linearity with maximum power efficiency is chosen. To characterize this, input power back-off (IBO) from the saturation power is introduced, and expressed as:

$$\mathrm{IBO_{dB}} = 10\log_{10}\frac{\mathrm{IP_{sat}}}{\widehat{\mathrm{P}}_{\mathrm{in}}} \qquad \text{Eq. II.20}$$

Where $\widehat{\mathrm{P}}_{\mathrm{IN}}$ the average input power and $\mathrm{P_{SAT}}$ the saturation output power.

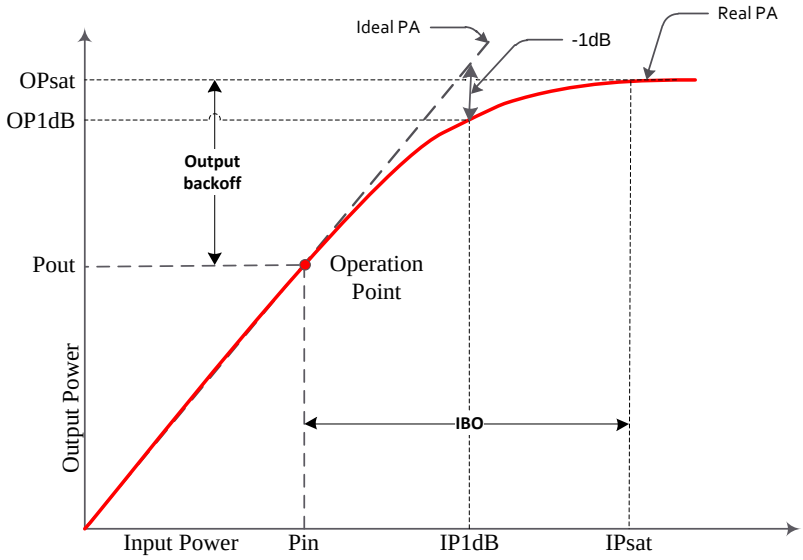


Figure II-22 Power Transfer Graph, 1 dB Compression Point and Saturation Power

Based on the simulation schematic of Figure II-23, Figure II-24 shows the effects of nonlinearity on single carrier with 16-QAM modulation where the constellation points are scaled differently. Hence, only the shape of the constellation is modified to circle-like shape. Whereas, in OFDM signal the signal experiences an additive distortion due to the subcarriers inter-modulation [5].

Table II.6 shows the signal-to-noise ratio penalties to achieve a BER of 10^{-3} for different input back-off (IBO) over Rician channels with K = 10 and 1. This data shows that SC-FDE is more robust compared to the OFDM due to the low PAPR of the single-carrier signal[1].

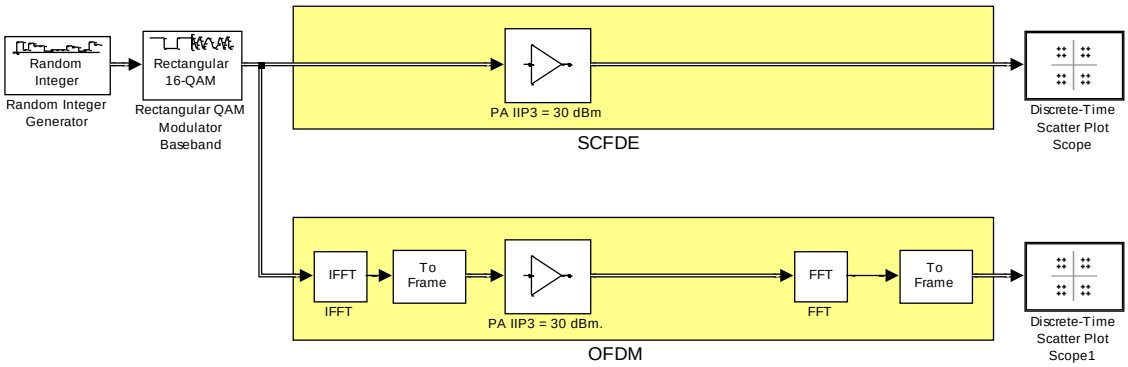
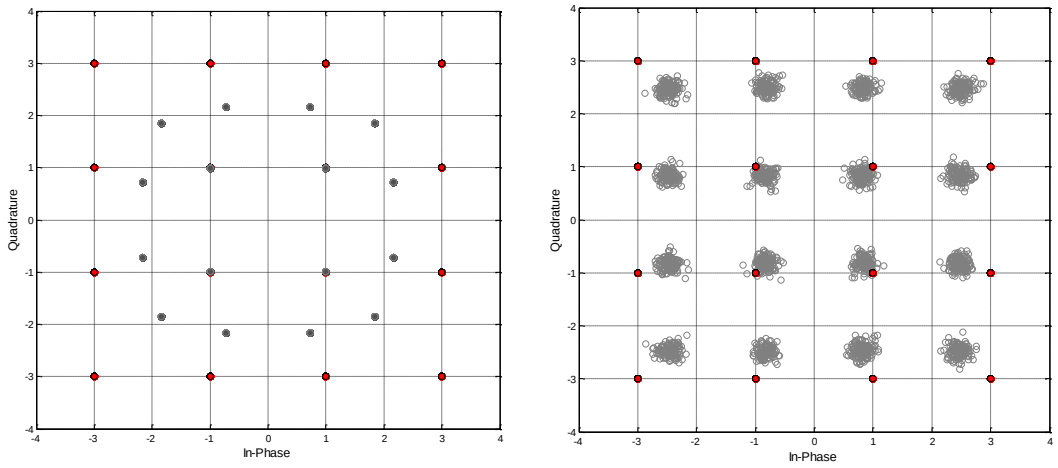


Figure II-23 Matlab Simulation of the Effects of the PA Nonlinearity on SC-FDE and OFDM Communication Scheme



SC-FDE OFDM

Figure II-24 The Influence of PA Nonlinearity with IIP3 = 30 dBm on the 16-QAM Constellation with SC-FDE and OFDM Communication Schemes

Table II.6 SNR Penalties at BER = 10^{-3} due to the PA Nonlinearity for Various IBOS [1]

Modulation Scheme		Rician Factor K = 10			Rician Factor K = 1		
		IBO = 8 dB	5	2	IBO = 8 dB	5	2
QPSK	OFDM	1.3	2.3	4.2	1.1	2.1	3.5
	SC-FDE	0.6	1.2	2.1	0.6	1.2	2.1
16-QAM	OFDM	2.1	5.8	-	1.6	3.9	-
	SC-FDE	0.7	1.3	2.2	0.7	1.3	2.2

II.6.2 Phase Noise from Local Oscillators (LOs)

Phase noise of an oscillator is the random fluctuations of its frequency; these random fluctuations are often modelled as random phase fluctuations on the system. In the 60 GHz RF frontends, phase noise generated by LOs is more serious since the phase noise of an oscillator increases at high oscillation frequency.

A local oscillator with phase noise process $\theta_{(t)}$affects the carrier signal $e^{j2\pi f_c t}$ and becomes $e^{j(2\pi f_c t + \theta_{(t)})}$. For free running oscillators, the phase noise is modelled as Weiner process that has a zero mean and the variance $\mathbb{E}\{\theta_{(t)}^2\} = \alpha t$, with parameter α depends on the quality of the oscillator [1].

The power spectrum density (PSD) of the phase noise process is given by:

$$S(f) = \frac{\alpha}{4\pi^2 f^2 + {\alpha}/{4}} \qquad \text{Eq. II.21}$$

The phase noise level of a LO is typically expressed in dBc/Hz at a certain offset from the carrier frequency f_c for a measured PSD.

From the simulation schematic of Figure II-25, Figure II-26 illustrates the effect of the phase noise of -60 dBc/Hz at 200 Hz on the 16-QAM constellation with SC-FDE and OFDM communication schemes over noise-free flat-fading channel. In case of SC-FDE the phase noise changes only the phase of the symbols, resulting in random phase rotations on the constellation. Whereas, in OFDM system the phase noise affects the orthogonality of the subcarriers that leads to inter-symbol interference (ISI) within data blocks and disturbance around the constellation become visible.

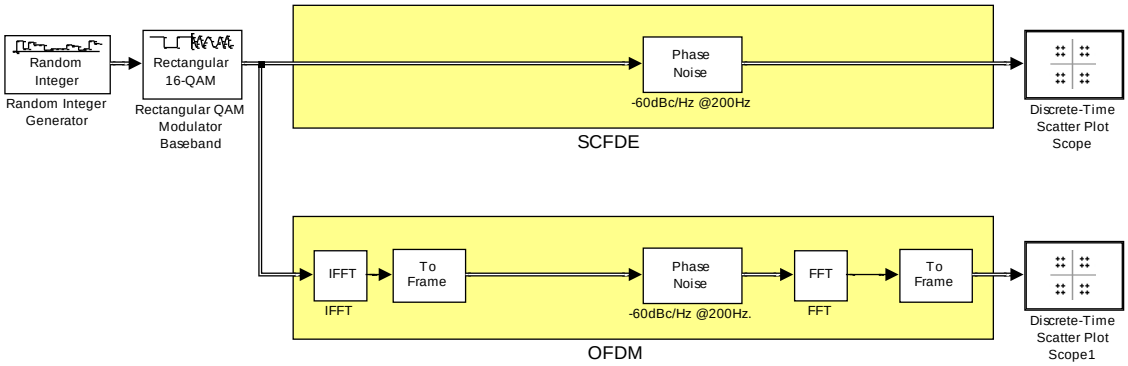


Figure II-25 Matlab Simulation Schematic of the Effects of the Phase Noise on SC-FDE and OFDM Communication Scheme

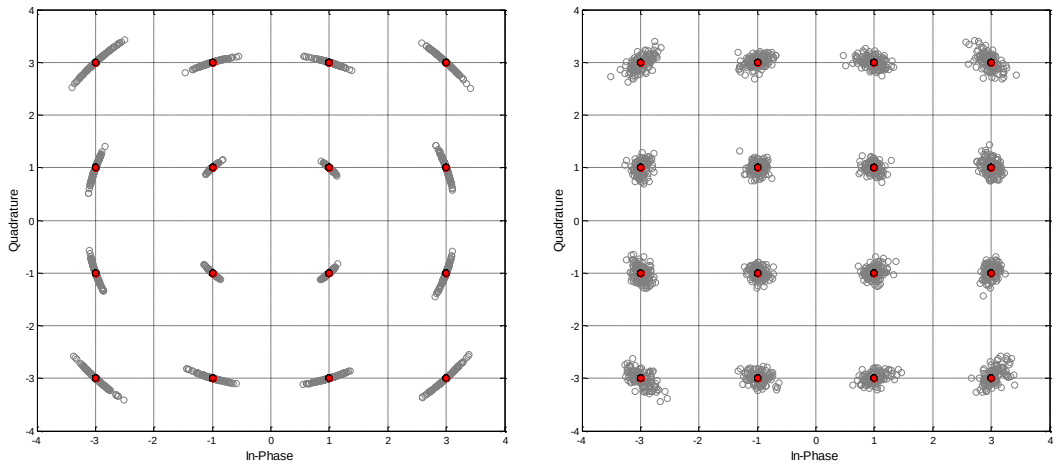


Figure II-26 Phase Noise Effect of -60 dBc/Hz on the 16-QAM Constellation with SC-FDE and OFDM Communication Schemes

II.6.3 IQ Mismatch and DC Offset

The IQ mismatch is defined as the phase/gain imbalances between I and Q branches in the quadrature modulator/demodulator due to the tolerance of RF components. This problem is particularly severe in direct-conversion frontend architecture because its

quadrature modulation/demodulation operates at much higher frequency than that of a super-heterodyne architecture [20].

The DC offset could originate from different analogue devices including amplifiers and RF mixers. Another important source of DC offset is the local oscillator self-mixing, where the LO signal may mix with itself down to zero IF due to the finite isolation between the LO and RF ports of the amplifiers and mixers [20].

As illustrated in Figure II-27, let's make α_I and α_Q the gains of I and Q branches, $\Delta\phi_M$ the phase offset of the two channels of the local oscillator. dc_I , dc_Q the dc offsets of the in-phase (I) and quadrature (Q) respectively. By making $Tx(t) = Tx_I(t) + jTx_Q(t)$ the complex baseband transmitted message, the output $\widetilde{T_x}(t)$ of an imbalanced modulator can be expressed as [21, 22]:

$$\tilde{T}_x(t) = M[T_x(t) + dc_M] \qquad \text{Eq. II.22}$$

Where:

$$Tx(t) = [Tx_I \quad Tx_Q]^T$$

$$dc_M = [dc_I \quad dc_Q]^T$$

$$M = \begin{bmatrix} a_I & -a_Q \sin(\Delta\emptyset_M) \\ 0 & a_Q \cos(\Delta\emptyset_M) \end{bmatrix}$$

At the receiver, the complex output $Rx(t) = Rx_I(t) + jRx_Q(t)$ of the imbalanced quadrature demodulator can be written as:

$$\tilde{R}_x(t) = D[\tilde{T}_x(t) + dc_D] \qquad \text{Eq. II.23}$$

Where:

$$\tilde{R}x(t) = \left[\tilde{R}x_I \quad \tilde{R}x_Q\right]^T$$

$$dc_D = [dc_I \quad dc_Q]^T$$

$$D = \begin{bmatrix} a_I & -a_Q \sin(\Delta\emptyset_D) \\ 0 & a_Q \cos(\Delta\emptyset_D) \end{bmatrix}$$

Taking into consideration the cascaded effect of both imbalanced modulator and demodulator the received baseband signal can be expressed as:

$$\tilde{R}_x(t) = DMT_x(t) + D[Mdc_M + dc_D] \qquad \text{Eq. II.24}$$

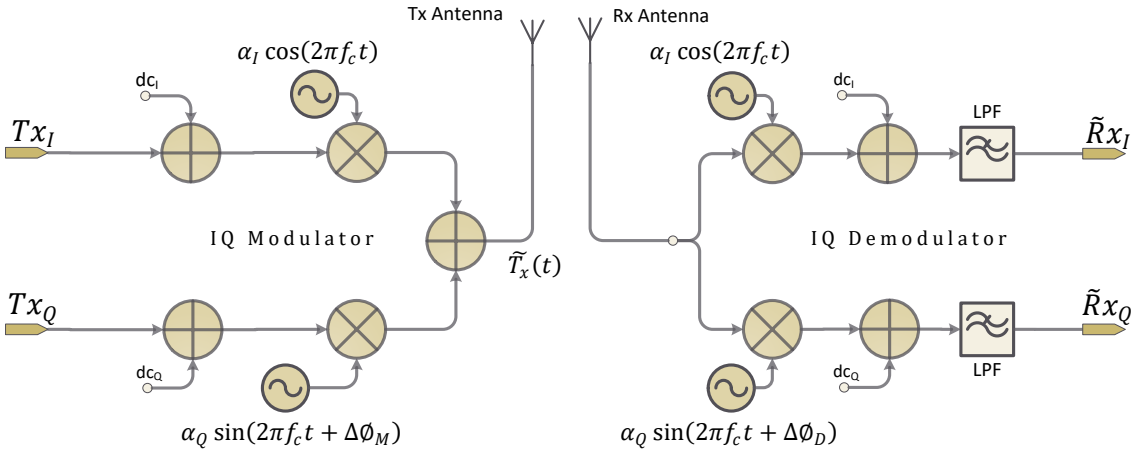


Figure II-27 IQ Mismatch in Modulator/Demodulator

The effect of the phase/gain imbalances on the 16-QAM constellation with SC-FDE and OFDM communication schemes is shown in Figure II-28, those imbalances have different effect on SC-FDE and OFDM communication schemes, in SC-FDE the imbalances changes the shape of the constellation to a trapezoidal, whereas in OFDM system each subcarriers are rotated and scaled differently [1].

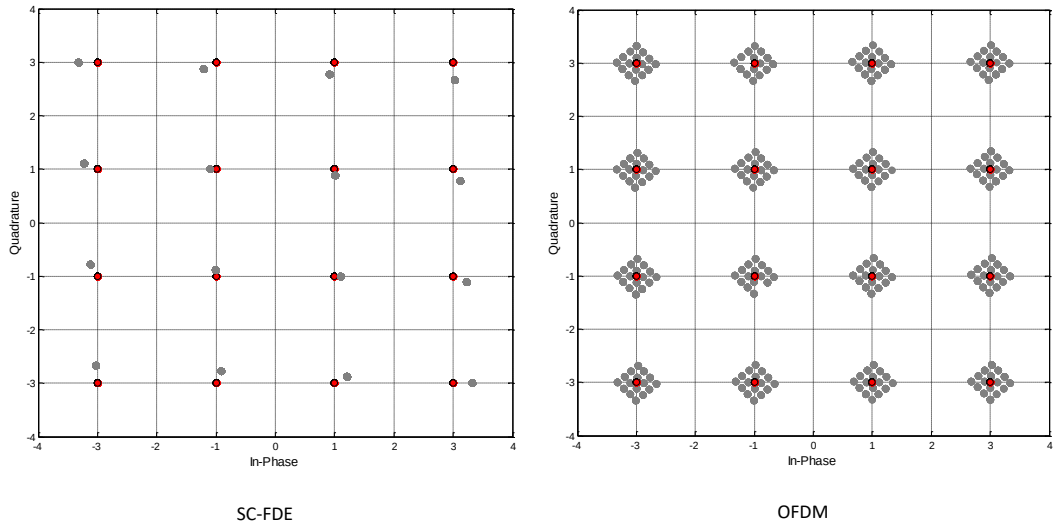


Figure II-28 Phase Imbalance of 6° Effect on 16-QAM Constellation with OFDM and SC-FDE

II.7 Conclusion

In this chapter, the 60 GHz frequency band characteristics and its potentials and challenges to realize reliable wireless personal area network (WPAN) were discussed.

We have presented a review of the 60 GHz indoor channel models, particularly the 60 GHz channel model adopted by the IEEE 802.15.3c channel modelling subcommittee, in which small-scale and large-scale fading were thoroughly discussed.

The baseband modulations adopted in the 60 GHz systems have been also investigated. The low-complexity binary modulation (e.g., OOK, MSK) shows high robustness against RF frontend imperfections, however, they have low spectrum efficiency and mainly reserved for low-cost applications. The SC-FDE and OFDM communication schemes, with M-ary modulations (e.g., 16-QAM, 8-PSK etc.), are the two solutions for Gb/s data-rate. The OFDM is adopted in bidirectional transmission over channels with high multipath severity. However, the OFDM suffers from high peak-to-average power ratio (PAPR) which makes it very sensitive to power amplifier nonlinearity. To overcome this weakness, single-carrier with frequency domain equalization (SC-FDE) presents a prominent alternative, where this technique has shown a comparable ability with OFDM to mitigate multipath effect in hostile radio propagation channel, but with much smaller peak-to-average power ratio and similar overall complexity.

Furthermore, the analogue RF frontends employed in 60 GHz wireless system have been introduced; the super-heterodyne and direct conversion architectures were studied along with their inherent RF impairments that characterize those frontends at the 60 GHz frequency. The effect of RF impairments on the performance of both SC-FDE and OFDM transmission techniques has also been discussed, and the robustness of SC-FDE compared to OFDM has been shown.

CHAPTER III
Software-Defined Radio

III.1 Introduction

As communications technology continues its rapid transition from analogue to digital, more functions of the modern radio systems are implemented in software, thus, leading towards the software radio. The concept of Software-defined radio (SDR) first appeared in 1995 with the work of Mitola [23], since, the SDR starts to be included in commercial and defence wireless radio systems. The SDR promises to increase flexibility, hardware lifetime, lower costs, and reduce time to market.

III.2 What is Software-Defined Radio?

So far, there is not a unique definition of a software-defined radio, different literatures give a variety of definitions, most common definitions are summarised as follows:

- Software-defined radio is a radio in which some or all of the physical layer functions are software-defined [24].
- Software-defined radio is a communication system that performs many of its required signal processing tasks in programmable digital signal processing (DSP) engine [25].
- Software Radio is an emerging technology, thought to build flexible radio systems, multi-services, multi-standards, multiband, reconfigurable and reprogrammable by software [26].

In our view of the software-defined radio, and with the respect to our aim to build a software-defined radio on a FPGA, the second definition is adopted. Therefore, SDR is defined as follows:

A software-defined radio is radio communication system that uses programmable digital devices to perform the signal processing necessary to transmit and receive baseband information at radio frequency.

III.3 Ideal Software-Defined Radio

The ideal software radio architecture shown in Figure III-1 consists of a digital system interfaced with the analogue frontend using analogue to digital converters (ADC) and digital to analogue converters (DAC). An ideal SDR has minimum analogue stages, and they are restricted to only those that cannot be performed digitally; the power amplifier (PA), the low noise amplifier (LNA) and the antenna. The degree of ideality of SDR is defined as the placement of the ADC/DAC converters with respect to the antennas [26, 27].

The ADC samples and digitizes the overall received signal spectrum to be processed by the digital signal processing receiver. The digital processing can be performed by a general purpose processors (GPPs), digital signal processors (DSPs), field programmable gate arrays (FPGAs) or application specific integrated circuit (ASICs); the technology used will depend on the required speed and flexibility.

Hardware resources and software codes are stacked in a layered architecture so that the hardware is completely abstracted away from the user's application. The middleware layer achieves this functionality by wrapping up the hardware into objects and provides a hardware-independent framework with an application programming interface (API). This architecture allows the rapid building of portable and powerful SDR applications without going deep into low-level hardware [28].

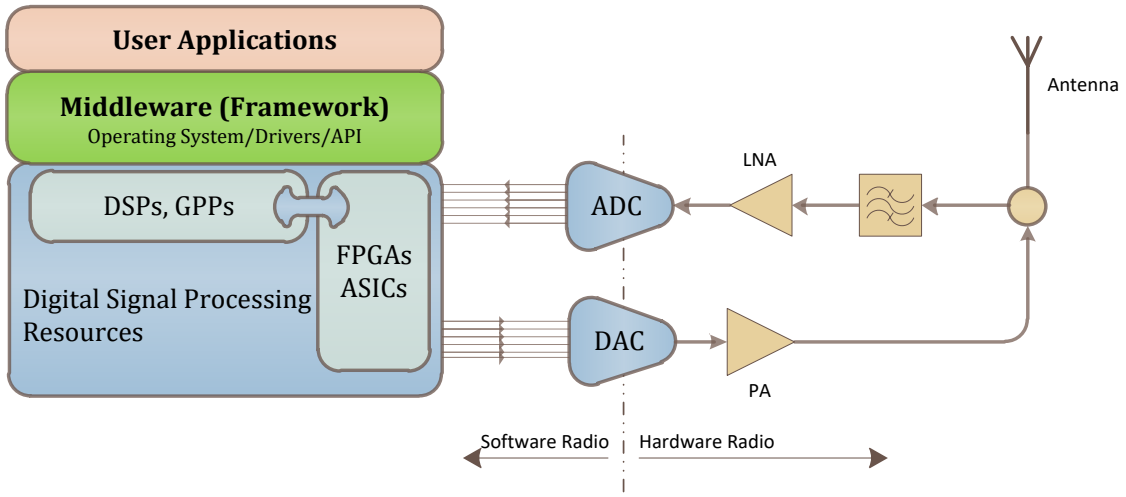


Figure III-1 Ideal Software-Defined Radio [28]

III.4 Benefits of Software-Defined Radio

The software-defined radio implementation can provide significant advantages summarized as follows:

- ❖ Provides high flexibility to implement many sophisticated radio systems without hardware constraints,
- ❖ Turning hardware problems into software problems making them easy to solve, (e.g., RF imperfections are easily compensated through digital signal processing),
- ❖ The hardware flexibility combined with software architectures making the SDR able to operate in multiples networks with different standards/protocols.

III.5 Software-Defined Radio Architecture

Considering the generalized SDR functional architecture of Figure III-2, this architecture is valid for either base station or handset terminal. The RF frontend converts one or more frequency bands of interest to digital intermediate frequency (IF) or baseband signal through a wideband ADC converter. The sampling frequency of the ADC converter defines the maximum allowable bandwidth of signal; hence, the maximum achievable data rate is directly related to the sampling rate of the employed ADC. The Antenna may include specialized processing supporting smart antenna, beam forming etc. The digitized signal is then processed by the digital frontend; this subsystem performs digital frequency tuning, channel selection and digital sample rate conversion to support the targeted air interface standard associated with the selected channel. The next stage is the baseband signal processing modem, this block performs different digital modulations/demodulations of the binary data. For forward error control, data conditioning module formats the user's raw data into frames and adds redundant bits [29]. Those modules mutually interact in order to be configured or parameterized to fulfil the PHY requirements of the targeted air interface.

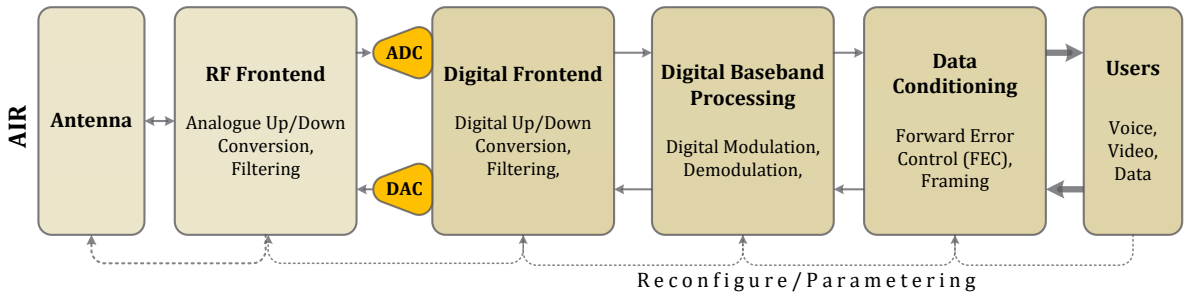


Figure III-2 Functional Architecture of a Software-Defined Radio

III.6 Radio Frequency (RF) Frontend

Historically, the notion of a frontend was applied to the closest stage of a receiver to the antenna. This stage gives access to the spectrum of interest, delivers a digital signal (ready for digital processing) at an intermediate frequency to the backend digital stages. However, with the introduction of software/digital radios a new definition of RF frontend has immerged [30], the RF frontend is considered as everything between the antennas and the ADCs/DACs converters, this includes all the analogue filters, low-noise amplifiers (LNAs), power amplifiers (PAs), and up/down-conversion mixers.

As shown in Figure III-3, the RF frontend receiver is basically a low noise amplifier (LNA) with a mixer to amplify and down convert the weak incoming RF signal and filters for image rejection. Hence, sensitivity and selectivity are the primary concerns in the receiver design. On the other hand, the RF frontend transmitter up converts and amplifies a baseband signal with a high power amplifier prior to transmission; in this case nonlinearity of the amplifier is a primary concern [30].

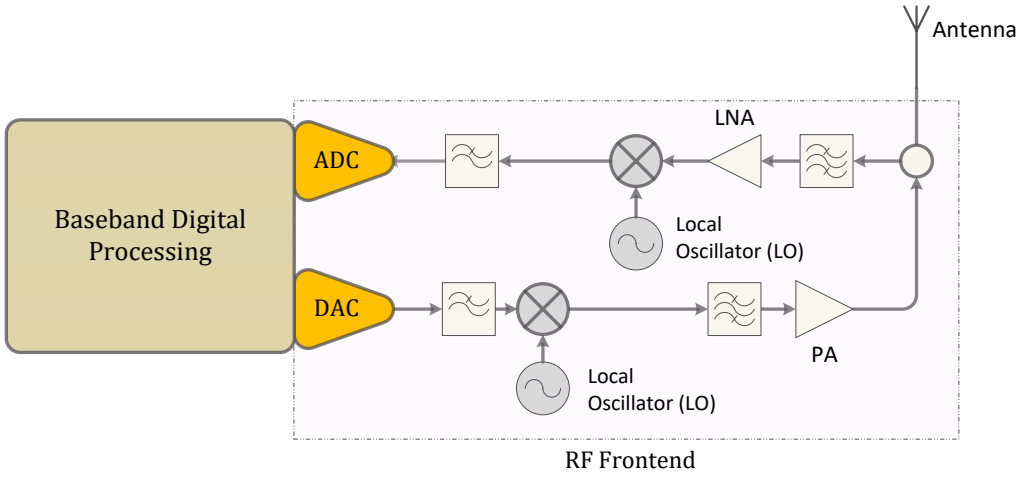


Figure III-3 RF Frontend of a Software-Defined Radio

III.6.1 RF Frontend Architectures

The most employed architecture is the well-known super-heterodyne topology, the super-heterodyne receiver as shown in Figure III-4.a uses a chain of low noise amplifiers, local oscillators, mixers and filters to down-convert, reject the images, limit the noise and select the desired channel's frequency. The super-heterodyne architecture uses at least two steps of mixing and filtering to recover the baseband signal. The first step mixes the signal down to an intermediate frequency (IF) that is fixed and independent of the desired signal centre frequency and the second step mixes the signal down to baseband [19]. Since most of the employed digital baseband modulations are phase modulated, the IQ mixer is employed to down convert the IF to IQ baseband components.

Another simplified version of the super-heterodyne is the homodyne architecture, called zero-IF or direct-conversion receiver. The down conversion (usually performed with IQ mixer) is carried out in one step without passing through the IF frequency as shown in Figure III-4.b. Compared to the super-heterodyne architecture, the direct-conversion receiver uses a reduced number of analogue components along with a reduction in power consumption. However, IQ mixers that operates at high frequencies risk self-mixing, where the local oscillator's leakage mixed with itself causes an important D.C. bias at the mixer's output [31].

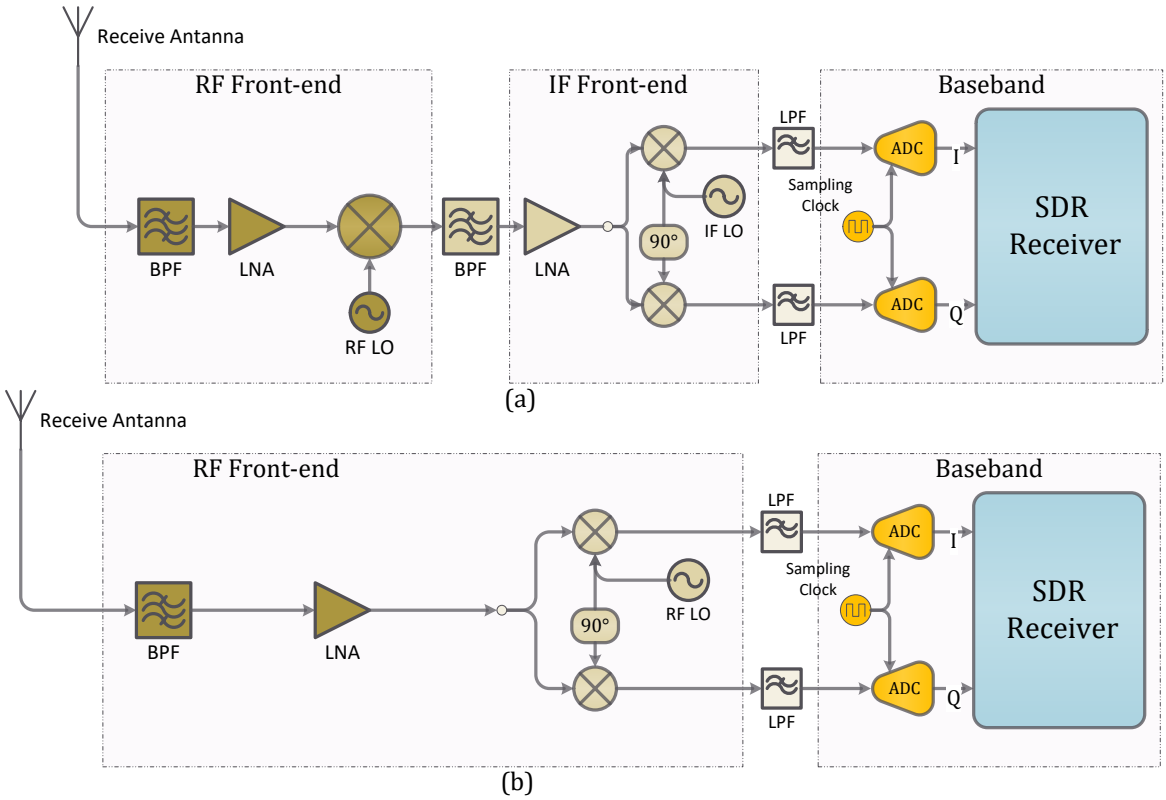


Figure III-4 Super-Heterodyne (a) and Homodyne (b) Architectures Receiver

III.6.2 Flexibility of the RF Frontend for SDR Radio

As defined in previous section SDR radio is required to adapt itself to different RF frequencies, bandwidth, and modulations. Unfortunately, the impossibility to implement the RF frontend components (i.e., PAs, LNAs, and RF Filters/Mixers) in software poses an obstacle to realize this goal. However, the parameters of the RF frontend (i.e., Gains, Filters frequencies, biases etc.) can be controlled and adapted by sophisticated software functions in order to reconfigure the RF frontend for handling multi-standards operation.

Due to the flexibility it offers, the direct-conversion frontend is an attractive option to realize this goal. Direct-conversion allows a wideband signal to be down converted through software. Furthermore, software compensation of the imperfections introduced by the RF frontend can be very beneficial. Figure III-5 illustrates a software controlled direct-conversion RF chain; in this case software handles the respective numbered tasks:

1. The transmitted signal can be accurately and easily pre-distorted with software functions to compensate for the power amplifier's nonlinearity, this can be achieved by adjusting the baseband signal level and monitoring the transmitted power to keep a linear response of the PA.

2. Feedback control of the receiver's gain for minimum noise and to provide the best signal-to-noise ratio for the ADC converter prior to digital signal processing,

3. Local oscillators can be tuned to select the targeted channel,

4. Biases and phase distortion of the IQ mixers can be identified and corrected through software.

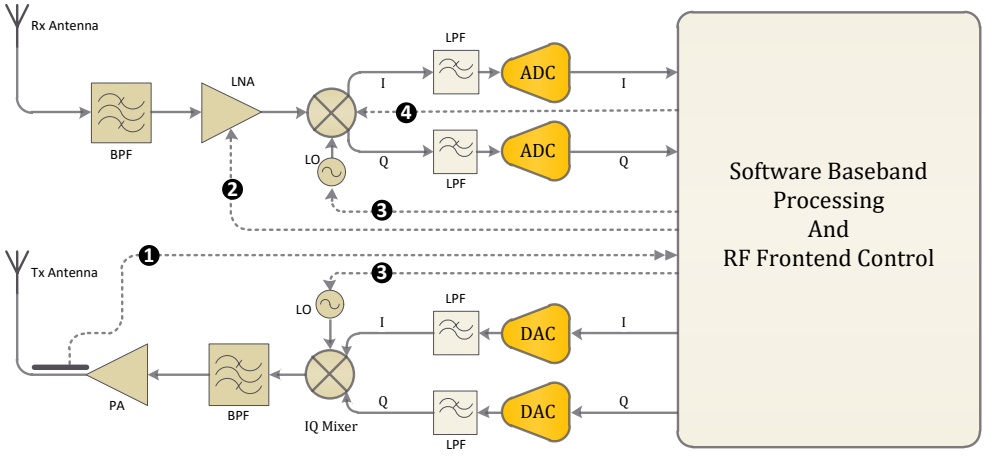


Figure III-5 Software Controlled/Adapted Direct-Conversion RF Frontend

III.7 Analogue to Digital Converters

The analogue-to-digital converter is one of the fundamental components of the software-defined radio. It is the most difficult component to select and the one that places the most constraints on Software-defined radio design. A trade-off must be made between real limitations such as sampling rate, dynamic range, ADCs resolution, and power consumption [31]. Figure III-6 shows a generic form of an A/D converter; it consists of an anti-aliasing filter, a sample-and-hold, a digitizer, and a buffer to hold the final converted digital value.

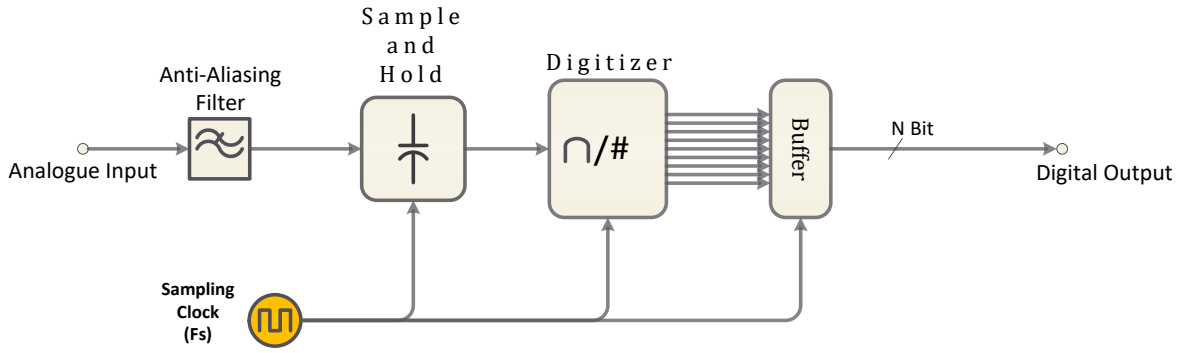


Figure III-6 Generic Form of an A/D Converter

Figure III-7 illustrates the output spectrum of the analogue signal sampled at a frequency F_s. The Nyquist sampling theorem states that the sampling frequency F_s, must be greater than or equal to twice the highest frequency component of the band-limited continuous signal $S_{(t)}$ ($F_s \geq 2F_d$), called Nyquist rate or the minimum sampling frequency that allows the integral digital reconstruction of the original signal .

When the sampling rate is smaller than the highest frequency component of the analogue signal ($F_s < 2F_d$), the frequency components that extent beyond the sampling frequency overlap on each other and causes a distortion on the signal, this is known as aliasing as shown in Figure III-7.b by the shaded regions [26].

Sampling the analogue signal at Nyquist frequency, (i.e., two times the cut-off frequency), requires an ideal anti-aliasing filter with a “brickwall” response to avoid spectrum overlapping, unfortunately these kind of filters are practically unrealizable. To overcome this constraint, the sampling frequency generally exceeds the Nyquist frequency ($F_s>2F_d$), well known as oversampling technique, in many cases this will be some integral multiple of the Nyquist frequency. A safety gap between the repeated spectrum images is left as shown in Figure III-7.b, and leads to a simpler anti-aliasing filter [28].

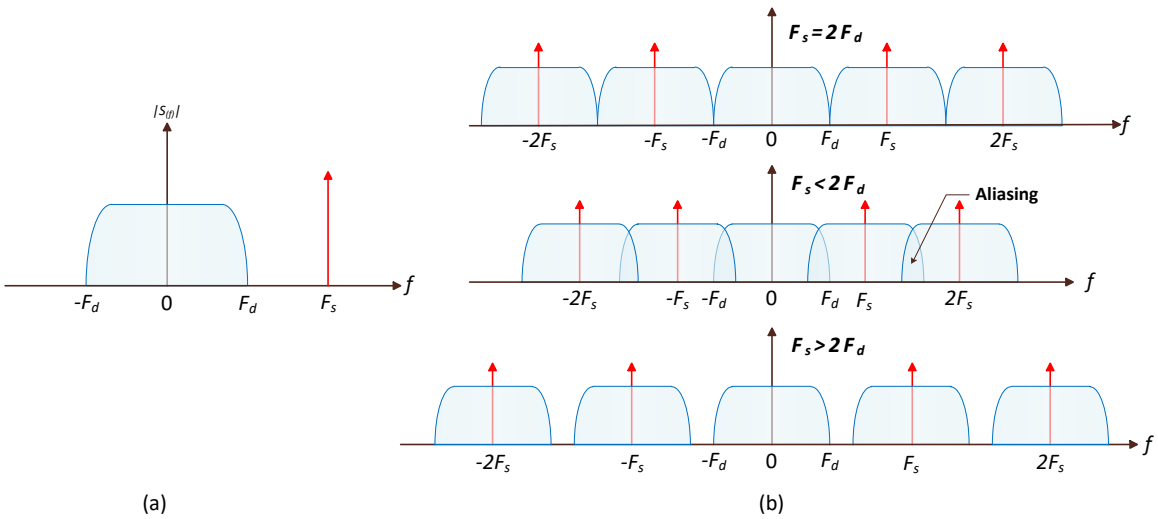


Figure III-7 Analogue Signal (a) and its Digitized Version Sampled at Frequency Fs (b)

III.7.1 Anti-aliasing Filter

As shown in Figure III-7, all frequency components above $F_s/2$ are aliased or folded back into the Nyquist zone, these include all unwanted components and noise. The analogue-to-digital converter must be preceded by an analogue anti-aliasing filter. This has the function of passing only the band of interest and rejecting all other unwanted frequency components. The low-pass and band-pass anti-aliasing filters are employed for the baseband and band-pass signal respectively [28].

III.7.2 Signal-to-Noise Ratio of ADCs

The process of quantization of both time and amplitude of the analogue signal, introduces several sources of error to the signal. The amplitude quantization step size q is directly related to number of bit B by:

$$q = \frac{V_{full}}{2^B - 1} \approx \frac{V_{full}}{2^B} \qquad \text{Eq. III.1}$$

Where V_{full} is the full-scale input voltage.

Considering a sinwave with full-scale peak-to-peak amplitude, the quantization error e is uniformly distributed in the interval $\pm q/2$; in this case the variance (i.e., power of the noise) of the quantization noise is given as follows:

$$\sigma_q^2 = \int_{-q/2}^{+q/2} e^2\, P(e) de = \frac{1}{q}\int_{-q/2}^{+q/2} e^2\, de = \frac{q^2}{12} \qquad \text{Eq. III.2}$$

With the power of the sinwave equals to $\frac{A^2}{8}$, the signal-to-noise ratio (SNR), at Nyquist rate, due to quantization noise of an ADC with B bit is as follows [28]:

$$SNR_{dB} = 10\log_{10}\left(\frac{A^2/8}{q^2/12}\right) = 6.02\,B + 1.76 \qquad \text{Eq. III.3}$$

The previous theoretical SNR was considered over Nyquist bandwidth (i.e. bandwidth of the signal is the same as the bandwidth of the sampling signal). Increasing the sampling frequency beyond the Nyquist bandwidth, spreads quantization noise power over wider band decreases the amount of the quantization noise within the Nyquist band [32]. Considering the sampling rate f_s, the SNR due to quantization noise can be expressed as:

$$SNR_{dB} = 6.02\,B + 1.76 + 10\log_{10}\left(\frac{f_s}{2f_{max}}\right) \qquad \text{Eq. III.4}$$

Oversampling the converted signal helps to compensate the lack of number of bits in the ADC converters. Since the actual ADCs technology provides very fast converters but with low resolution (i.e. 8 bits or less) [33].

III.7.3 Spurious Free Dynamic Range (SFDR)

Spurious Free Dynamic Range (SFDR) is the ratio of the peak power of the fundamental signal to the peak power of the largest spurious spectral component. SFDR is an excellent metric to show the fidelity of the ADCs particularly in software-defined radios. It is a more important specification than SNR because it encapsulates linearity and quantization noise performance.

Numerous sources of spurious components can be summarized but not limited to:

- Non-Ideality of anti-aliasing filter,
- Sample-and-hold, op-amps and digitizer nonlinearity,
- Spurious components of the sampling clock,
- Adjacent channels noise.

Figure III-8 shows a snapshot of the output spectrum of an ADC, the ADC conversion generates numerous spurious components within the Nyquist band. Thus, the spurious free dynamic range (SFDR) indicates the lowest power input signal that can

be distinguished from spurious signals. Any signal below the SFDR cannot be reliably identified as a true signal instead of as a spurious one. The generated spurious signals limit the sensitivity of an SDR receiver to low signals and even mask the desired signals.

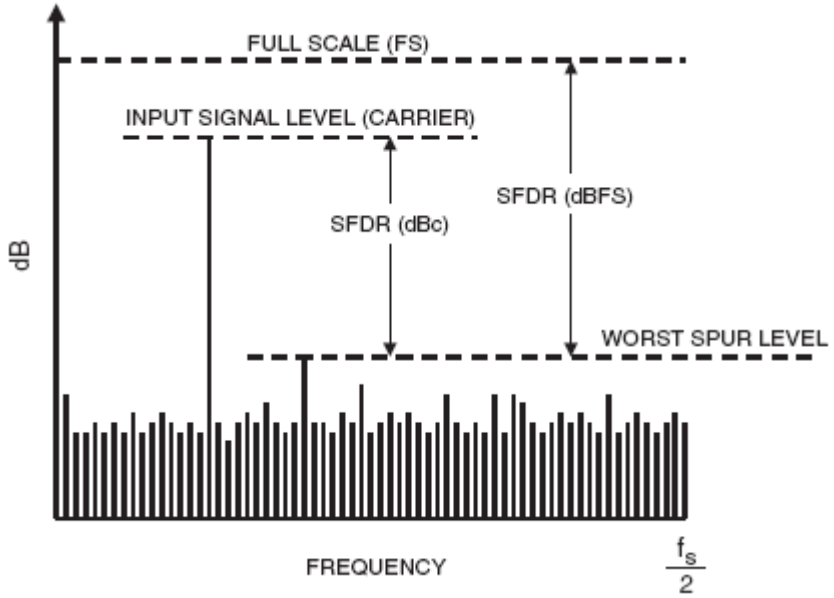


Figure III-8 Spurious Free Dynamic Range of an ADC

III.7.4 Band-pass Sampling

When the signal to convert is a band-pass signal, defined as a signal with no frequency components bellow a certain frequency F_{low} and above a certain frequency F_{high} and centred around F_c as shown in Figure III-9.a. The required sampling rate for an exact reconstruction of such band-pass signal is between at least two times the bandwidth F_{high}-F_{low} and two times the highest frequency of the band-pass signal, in other word the sampling frequency F_s must satisfy [32]:

$$\frac{2f_{high}}{k} \leq f_s \leq \frac{2f_{low}}{(k-1)} \qquad \text{Eq. III.5}$$

Where k is an integer that satisfy:

$$2 \leq k \leq \frac{f_{high}}{(f_{high} - f_{low})} \qquad \text{Eq. III.6}$$

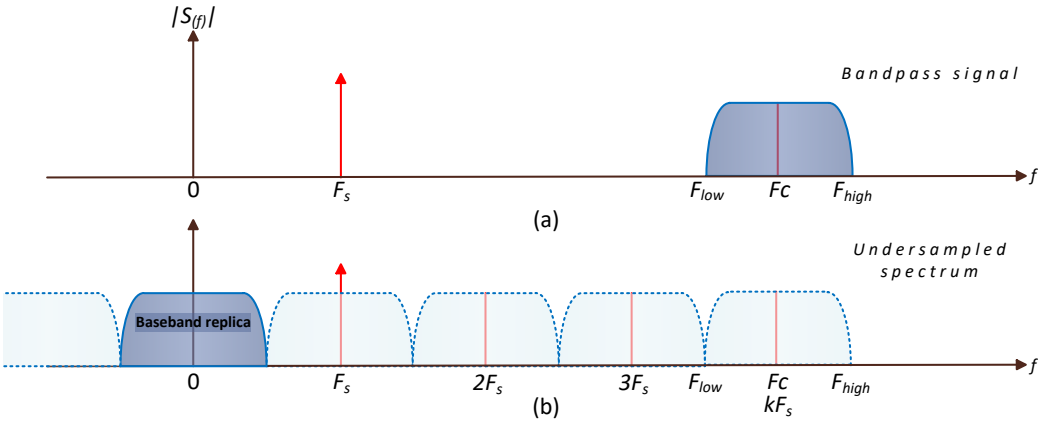


Figure III-9 Band-pass Signal (a) and its Under-Sampled Spectrum (b)

As shown in Figure III-9.b the sampled spectrum of the band-pass signal consists of multiple replicas of the original signal that are repeated at integer multiples of the sampling frequency. By selecting the appropriate spectral replica of the original band-pass signal a down-conversion function can be realised. The principle of band-pass sampling is to sample the centred band-pass signal of bandwidth $W_{Nyquist}$ at frequency kf_s (k≥2, k is even) at the Nyquist rate f_s [26].

Known as the under-sampling technique, this method offers a down-conversion of the high frequency RF or IF signal to complex baseband, thereby reducing the need for an additional analogue down-conversion stage prior to sampling or a digital conversion stage following the sampling.

III.7.5 Quadrature Sampling

When complex modulation is used (e.g., QPSK, 16-QAM, PSK etc.) in which both in-phase (I) and quadrature (Q) components are modulated. As shown in Figure III-10, at the receiver the IQ pair can be respectively recovered by mixing the modulated carrier with the reference local oscillator and the 90° shifted reference. If the complex carrier has a Nyquist frequency equals to Fs, the real (I) and the imaginary (Q) components can be sampled independently by a half of the original Nyquist frequency F_S [26].

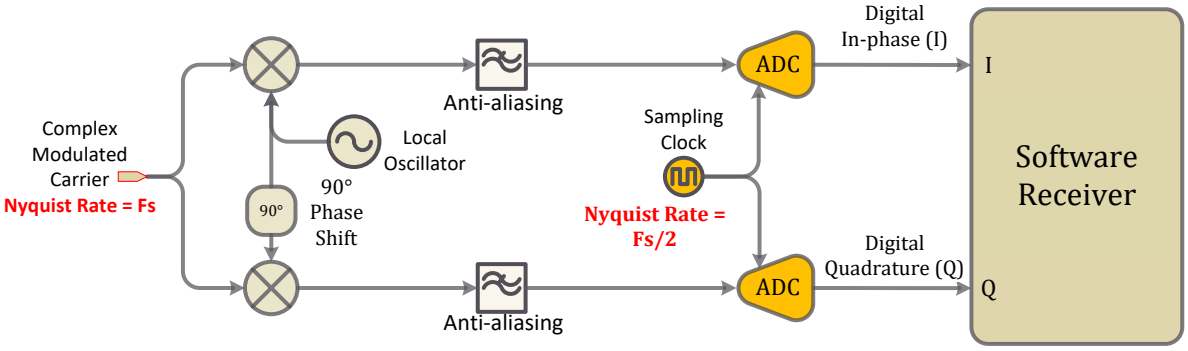


Figure III-10. Quadrature Sampling Technique

III.8 Digital to Analogue Converters

The digital to analogue converters (DACs) are specifically used in the transmitter to reconstruct one or multiple carriers that have been digitally synthesized and modulated into a continuous-time signal. In the reconstruction process the no ideal characteristics of the DAC (quantization noise and spurious components) yield to unpredictable results. It is the performance of the DAC that determines whether particular modulation scheme or system architecture can meet the specifications.

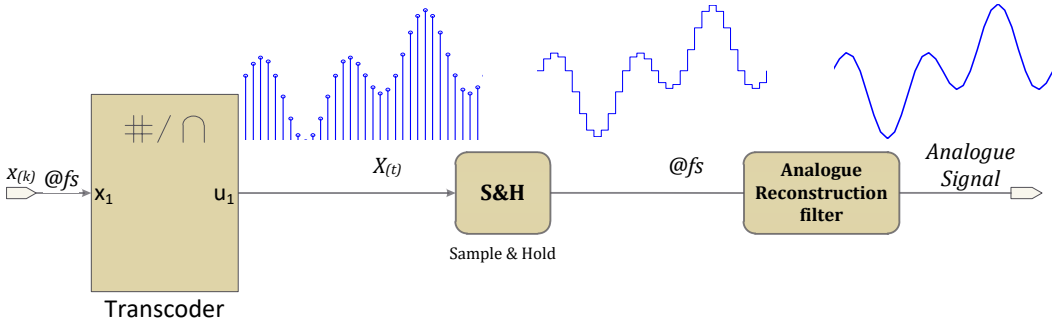


Figure III-11 Digital to Analogue Converter and Reconstruction Process

As shown in Figure III-11 the reconstruction operation is obtained by the cascade of a sample and hold (S&H) and a filter after that the digital value is translated into an analogue voltage by the transcoder. The S&H generates a staircase-like waveform; in the frequency domain this waveform is an infinite replica of equal spectra that repeats every f_s. The reconstruction filter smoothers the staircase-like waveform by completely removing the replicas, leaving the band-base unchanged [34]. Ideally, reconstruction uses a filter with transfer function:

$$H_{(f)} = \begin{cases} 1 & for\ -\frac{f_s}{2} < f < \frac{f_s}{2} \\ 0 & otherwise \end{cases} \qquad \text{Eq. III.7}$$

The performance of DACs in wireless systems is often analysed in the frequency domain, where the out-of-band noise and spurious components that fall outside the channel bandwidth but inside the DAC Nyquist bandwidth are characterized [19].

Compared to the power of the transmitted signal, the quantization noise generated by a DAC is generally not important. However the out of band spurious components will be radiated and can cause unwanted inter-modulation that appears inside the bandwidth of the receiver [33]. Figure III-12 shows the spurious components of the AD9772A DAC converter with single-tone signal. The allowable spurious emissions mask will depend upon the air interface standard. E.g., for CDMA2000 base stations with a power output greater than 33 dBm (2W), spurious responses greater than 1.98 MHz from the carrier must be less than 60 dB below the carrier power [28].

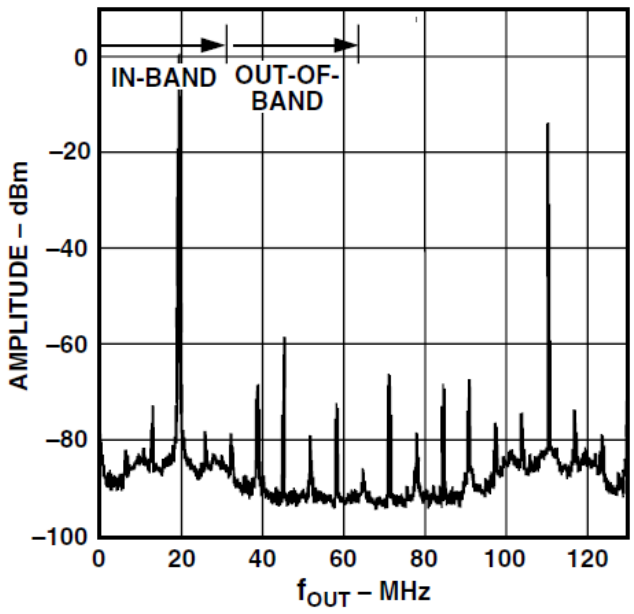


Figure III-12 Single-Tone Spectral Analysis of AD9772A DAC with F_{data} = 65 MHz

III.9 Digital Frontend

Mainly derived from the radio frequency (RF) frontend and digital signal processing, the digital frontend performs the frontend functionalities (i.e., up/down conversion, channel filtering) digitally [35].

At the transmitter, the digital frontend provides a digital baseband/IF signal at certain bandwidth W_b, centre frequency f_c and samples rate F_s that fulfil the Nyquist criterion $F_s \geq 2W_b$. The synthesized digital signal is then converted to analogue format before being up-converted to a higher RF frequency by the transmitter's RF frontend prior to transmission.

At the receiver, the inverse process is performed, where after digitizing the down-converted RF signal (i.e., baseband or IF signal) with wideband ADCs. The digital frontend of the receiver down-converts and filters the signal of interest to a digital baseband signals. This process is performed along with a sample rate conversion (usually down-sampling) to the minimum rate. In addition, due to that the final frequency and sampling translation is performed in the digital frontend, the frequency and timing synchronization are usually considered as a part of the digital frontend.

Figure III-13 illustrates a common structure of the transmitter/receiver digital frontends, having the same functionalities as the RF frontend. Similar to its analogue counterparts (analogue mixer, local oscillator, and filters), numerically controlled oscillator (NCO), digital mixers and digital filters perform the frequency translation and filtering of the received digital signal. A frequency error feedback tunes the NCO's frequency to compensate any frequency offsets, and timing error sets the sampling instant to compensate any timing errors of the ADC converter.

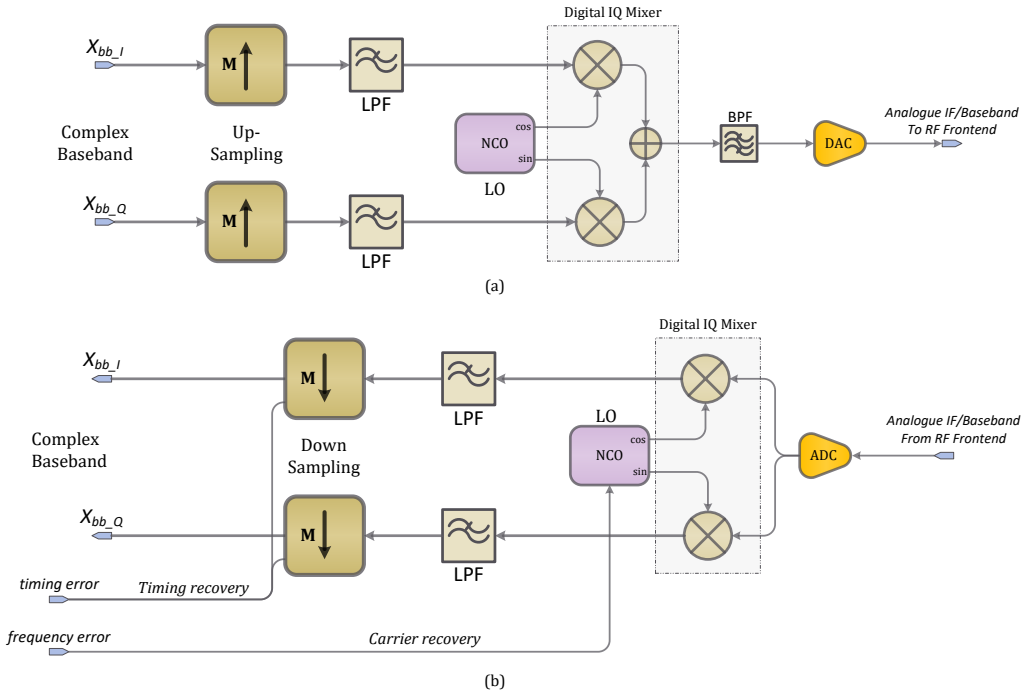


Figure III-13 Transmitter (a) and Receiver (b) Digital Frontend

III.9.1 Direct Data Synthesizer (DDS)

A direct digital synthesizer (DDS) is an important component in any digital communication system. DDS is used for constructing an arbitrary digital signal, usually used to generate a sinwave signal (i.e., to replicate the Local Oscillators used in Hardware Radios); DDS can be employed to implement different type of modulations schemes (e.g., phase and frequency shift keying modulations).

Unlike analogue synthesizers, DDS have the advantages of high precision, very low spurious components, fast switching, small size and low cost that makes it attractive solution for mobile application. However, DDS's frequency is limited by the Nyquist rate (i.e., $f_{max} \leq \frac{f_{clk}}{2}$, f_{clk} the system clock) making them impossible to implement above the very high frequency [31].

A numerically controlled oscillators (NCO) is a DDS that generates sine and cosine waveforms, mainly used in quadrature digital up/down converters. Figure III-14 shows the common structure of NCO that employs a lookup table scheme for digitally generating a complex and real valued sinusoid. Implemented on a read only memory (ROM), the lookup table (LUT) stores the digital samples' values of the synthesized sinusoid (usually uniformly spaced). This ROM is addressed by a phase accumulator

clocked by the system clock of frequency F_s, this accumulator increments the LUT's address by Δθ at each clock cycle.

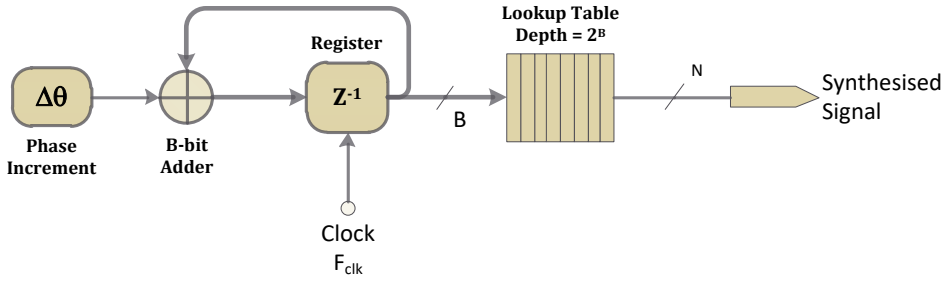


Figure III-14 Lookup-Based Numerically Controlled Oscillators (NCO)

The frequency of the synthesized sine wave f_{out}, is a function of system clock f_{clk}, the number of bits in the accumulator B and phase increment Δθ [36]:

$$f_{out} = \frac{f_{clk}\Delta\theta}{2^B} \qquad \text{Eq. III.8}$$

The purity, in other word the spurious free dynamic range (SFDR) of the signal is affected by both the phase and amplitude resolution. The depth B and width N of the LUT effects the phase resolution and the amplitude resolution of the signal respectively. These limited resolutions, add spurious components and white noise floor to the signal's spectrum. Figure III-15 illustrates the SFDR of a NCO implemented with Xilinx IP-Core with 10 and 20 Bit LUT depth and width respectively; the generated signal has the frequency of 0.22825×f_{clk} and -118 dB SFDR.

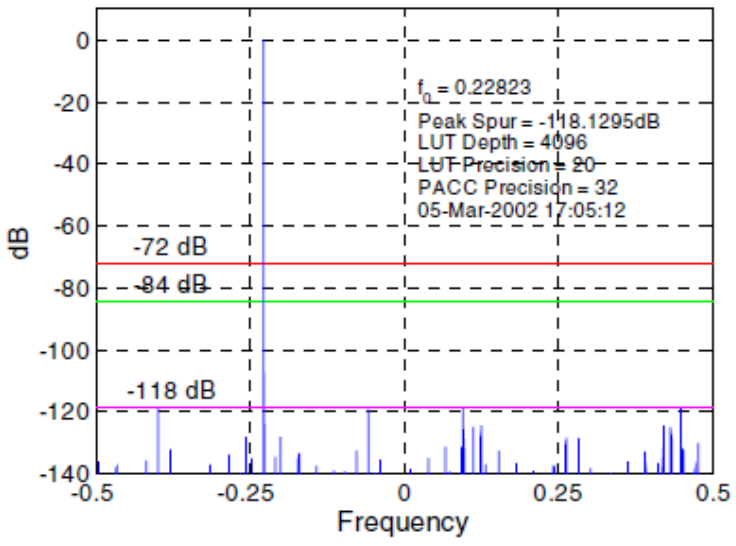


Figure III-15 SFDR of the Synthesized Single Tone Signal of a NCO with B =10 Bit and N = 20 Bit

III.9.2 Digital Up/Down Converter (DUC/DDC)

The digital up/down conversions (DUC/DDC) perform the digital frequency conversion function to link the baseband processing function with the RF frontend. Mainly, it's referring to shift of a signal's spectrum towards higher or lower frequencies respectively. DUC and DDC can be achieved by digitally multiplying the signal $x_{(nT)}$with a complex carrier $e^{j2\pi f_c nT}$ (synthesized by NCO), where f_c is the frequency shift (generally called carrier frequency), and T the sampling period. Depending on the sign of f_c, up-conversion and down-conversion is achieved by the following complex multiplication [19]:

$$x_{out_{(nT)}} = x_{in_{(nT)}} \times e^{j2\pi f_c nT} \qquad \text{Eq. III.9}$$

The Eq. III.9 formulates DUC/DDC as complex multiplication. However, real multiplication is possible by multiplying the signal with a sine or cosine function instead of the complex exponential of Eq. III.9. Writing the complex baseband signal with its in-phase (I) and quadrature (Q) components, the real up-conversion of the baseband $x_{BB} = I + jQ$ to the RF signal T_x is performed as follows:

$$T_{\mathrm{x}} = \Re_e\{x_{BB,Tx} \times e^{j2\pi f_c nT}\} = I_{Tx}\, cos(2\pi f_c nT) + Q_{Tx}\, sin(2\pi f_c nT) \qquad \text{Eq. III.10}$$

The above equation can be written in different way:

$$T_{\mathrm{x}} = \Re_e\{x_{BB,Tx} \times e^{j2\pi f_c nT}\} = \frac{1}{2}\left(x_{BB,Tx} \times e^{j2\pi f_c nT} + x^*_{BB,Tx} \times e^{-j2\pi f_c nT}\right) \qquad \text{Eq. III.11}$$

The Eq. III.11 shows that the output signal of the up-conversion contains two components, one centred at f_c and another centred at $-f_c$. Hence, an analogue band-pass filtering is applied to get rid of the negative image prior to transmission. Figure III-16.a shows a digital up-conversion.

At the receiver, and in order to recover the two components I_{Rx} and Q_{Rx} of the baseband signal $x_{BB,Rx}$, a real multiplication of the received signal with the sine and cosine components of the NCO of frequency $-f_c$ is as follows:

$$\boldsymbol{I_{Rx}} = \Re_e\{x_{BB,Tx}e^{j2\pi f_c nT} \times \cos(-2\pi f_c nT)\} = \boldsymbol{I_{Tx}} + I_{Tx}\cos 2\pi(2f_c)nT - jQ_{Tx}\sin 2\pi(2f_c)nT \quad \text{Eq. III.12}$$

$$\boldsymbol{Q_{Rx}} = \Re_e\{x_{BB,Tx}e^{j2\pi f_c nT} \times \sin(-2\pi f_c nT)\} = \boldsymbol{Q_{Tx}} + Q_{Tx}\cos 2\pi(2f_c)nT + jI_{Tx}\sin 2\pi(2f_c)nT \quad \text{Eq. III.13}$$

Eq. III.12 and Eq. III.13 show that the transmitted baseband signal can be easily recovered by simply apply a low-pass filtering to removes the high frequency components as shown in Figure III-16.b.

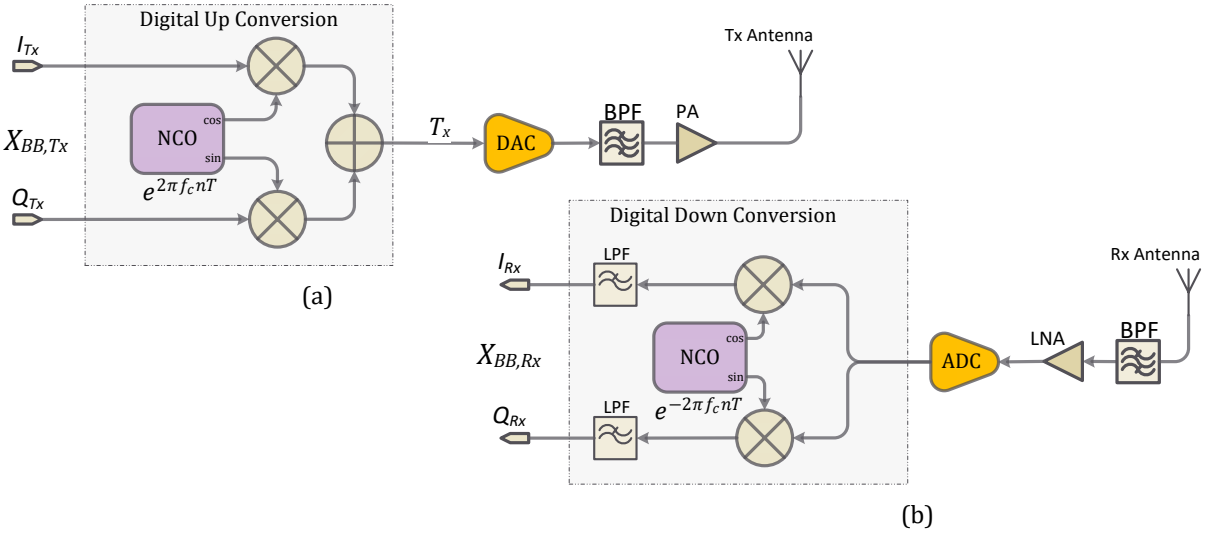


Figure III-16 Digital Up/Down Conversion

III.9.3 Sample Rate Conversion

Given that different wireless standards are based on different sample/chip-rates, it is necessary to perform digital signal processing at different clock-rates. The straight forward solution is to clock the ADCs at tuneable frequency. However, generating variable frequency signal with high stability (low jitter) is very costly. Re-sampling is the method of changing the sample-rate without altering the signal's content by applying up-sampling or down-sampling [37]. A digital signal $x_{(nT)}$ is up-sampled (i.e., interpolation) to a higher sampling rate or down-sampled (i.e., decimation) to a lower sampling rate.

III.9.3.1 Up-Sampling (Interpolation)

When up-sampling is performed, new samples are inserted into the original signal. The up-sampling is mainly employed in the transmitter by transforming the modulated signal to a higher resolution to match the sampling rate of digital up-

conversion (DUC) and to relax the requirements of the reconstruction filters after DAC conversion [31].

Figure III-18 illustrates an up-sampling mechanism by a factor of two of a digital signal. In the frequency domain the up-sampling introduces high frequency images, those images should be removed or at least attenuated through a low-pass filter before any up-conversion or digital to analogue conversion; as shown in Figure III-18.

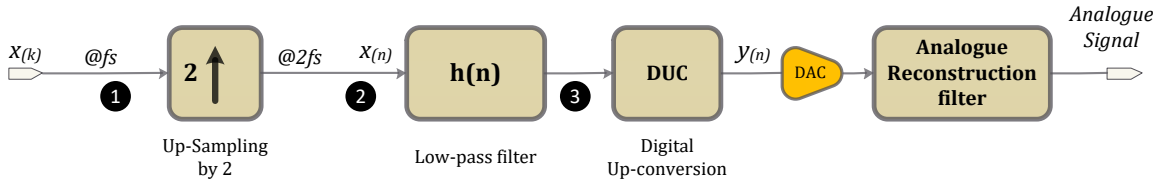


Figure III-17 Filtering after Up-Sampling

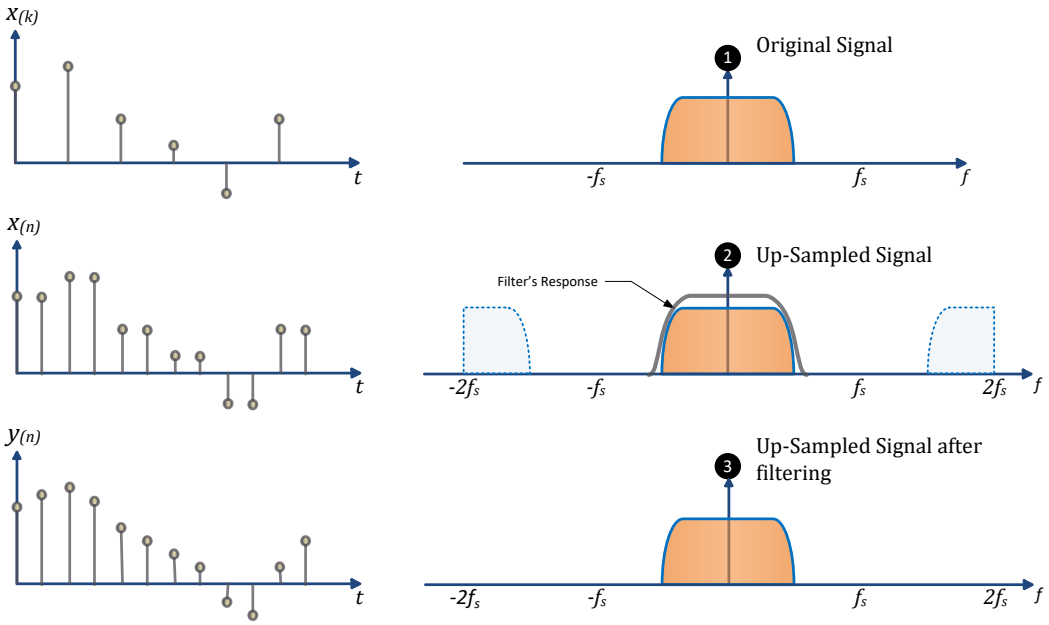


Figure III-18 Time and Frequency Domain Presentation of Up-Sampling

III.9.3.2 Down-Sampling (Decimation)

The down-sampling operation of a digital signal is the process of reducing the sampling rate of a high-rate signal to a lower rate without corrupting the content of the original signal. As shown in Figure III-19, the re-sampling of the signal at lower sample-rates is generally employed at the receiver after any analogue to digital conversion or after digital frequency down-conversion to reduce the requirements (memory size and bandwidth) of the signal processing stages.

As shown in Figure III-20, the down-sampled signal $y_{(m)}$ by a factor of D can be obtained by selecting one out of D samples of $x_{(n)}$ and discarding the other D-1 samples. In the frequency domain the down-sampling decreases the bandwidth of the original signal. As long as the aliasing (overlapping of images) is avoided, the spectrum content of the down-sampled signal it's not altered. For this purpose, the down-sampling is usually preceded by a low-pass filter to avoid aliasing of the lowered rate signal by respecting the Nyquist-rate limit [38].

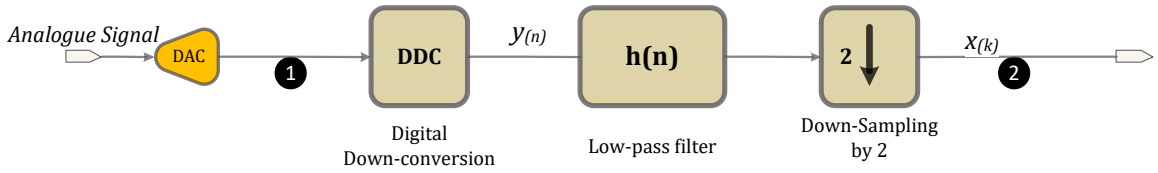


Figure III-19 Filtering Before Down-Sampling

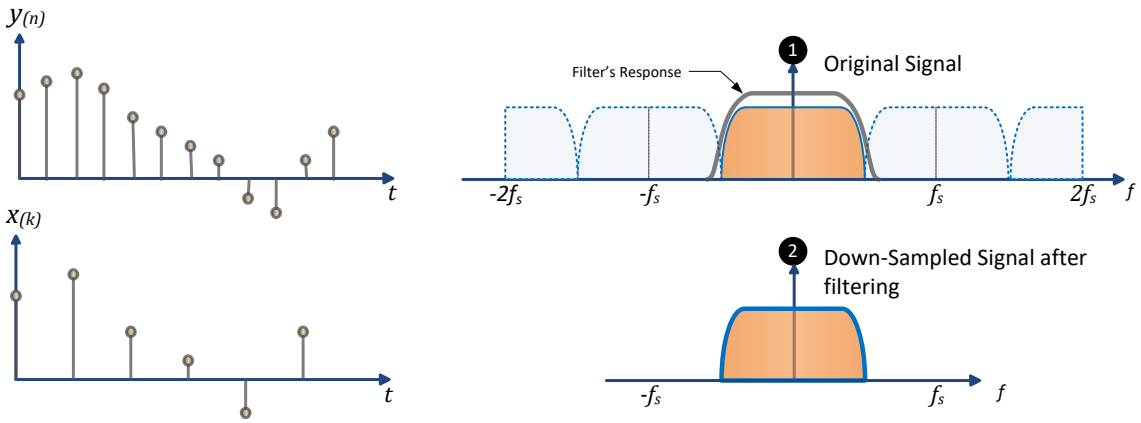


Figure III-20 Time and Frequency Presentation of Down-Sampling

III.9.4 Sample-Rate Conversion by a Non-Integer Factor

In some practical scenarios the up-sampling/down-sampling factor is rational factor N/M, Basically, we can achieve this sampling rate conversion by first performing up-sampling by an integer factor N and then down-sampling the interpolated digital signal by an integer factor M. In other words, a sampling rate conversion by the rational factor N/M is accomplished by cascading an interpolator with a decimator with a common anti-aliasing filter employed between the two processes as illustrated in Figure III-21 [39].

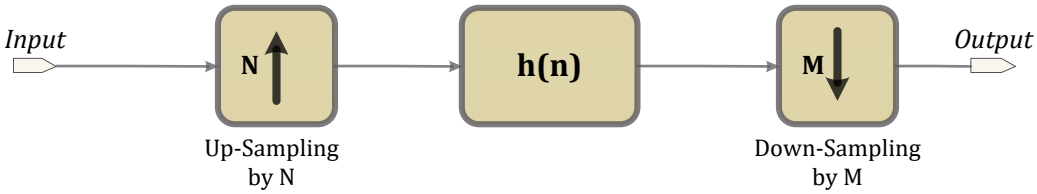


Figure III-21 Sample-Rate Conversion by a Rational Factor N/M

III.10 Digital Filters

Most digital filter designs are either infinite impulse response (IIR) or finite impulse response (FIR). IIR filters have impulse responses that are infinite and FIR filters have ones that are not. FIR filters are intrinsically stable because they do not incorporate feedback, the IIR filters have feedback so the choice of coefficients has an impact on the stability and it is impossible with an IIR filter to achieve a linear phase response. However, IIR filters require less number of coefficients than FIRs with similar frequency response, which means FIR consumes more resources. Since information is carried by both amplitude and phase in digital communications systems, the IIR filter is generally avoided, Figure III-22 shows the structure of the two designs [28].

The degree to which the filter response matches the ideal response is dependent on two parameters: the oversampling factor M and number of taps N. Generally, N is chosen to be an integer multiple of M, the number of taps N (filter order) is given by: N=D×M, D is an integer value [40].

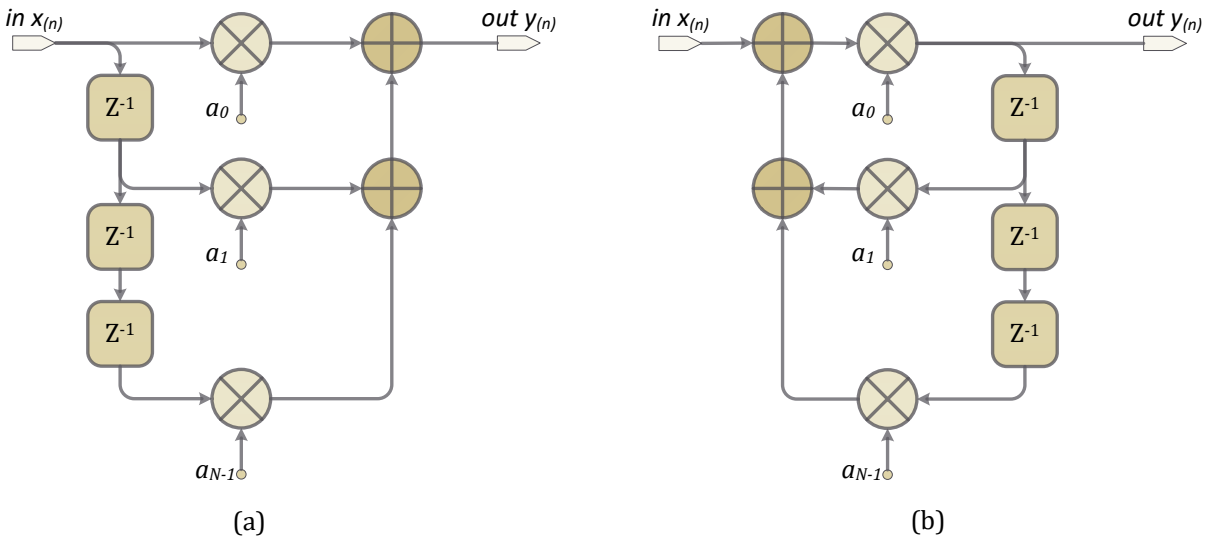


Figure III-22 Finite Impulse Response (a) and Infinite Impulse Response (b) Filters

III.11 Cascaded Integrator Comb (CIC) Filters

In software-defined radios, sample rate changes can be very large. To achieve this sample rate conversion, digital filters such as FIR requires a very high number of multipliers that are complex and power-hungry [28].

Cascaded integrator comb (CIC) filters are a popular choice that efficiently performs filtering along with decimation and interpolation. CIC filters are flexible, multipliers-free, and suitable for implementation in hardware and handle large sample-rate arbitrary changes. As its name indicates, CIC is a cascade of simple integrators (accumulators) and a cascade of comb filters (delay and subtract from the current sample) [31]. Integrators and combs schematic are shown in Figure III-23.

Figure III-23 Building Block of CIC Filter

The CIC decimator filter is a cascade of integrators, decimation, and combs. The CIC interpolator consists of cascaded combs, interpolation, and integrators as shown in Figure III-24.

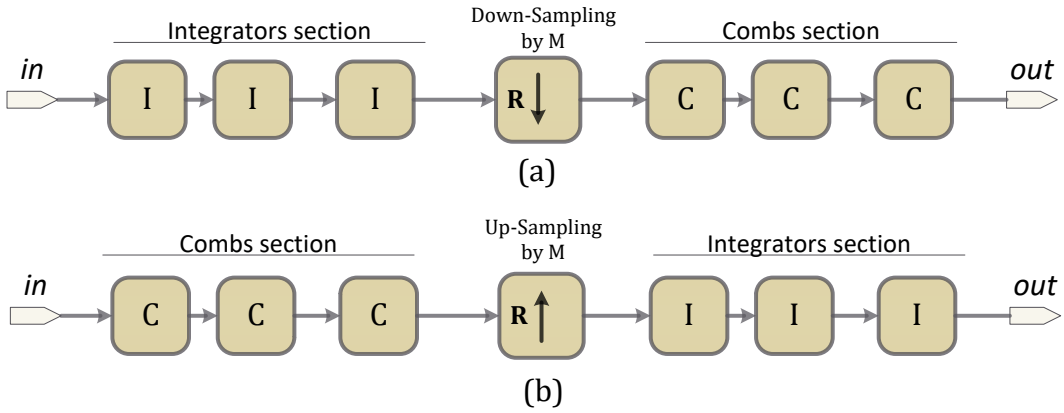


Figure III-24 CIC Decimator (a) and Interpolation (b) Filters

The transfer function of the CIC decimator respective to the higher sample rate with N integrators/combs, M samples deferential delay in the combs (usually M = 1 or 2), and decimation factor of R is written as follows:

$$H_{(z)} = \left(\frac{1 - z^{-RM}}{1 - z^{-1}}\right)^{N} \qquad \text{Eq. III.14}$$

Figure III-25 plots the magnitude response of a CIC decimation filter, with 4 integrator/comb stages, M=1 and decimation factor of 5. This low-pass filter has a cut-off frequency f_c that is directly related to the width of the aliasing band, which is the frequency band that folds onto the pass-band region (i.e., around zero hertz) after decimation.

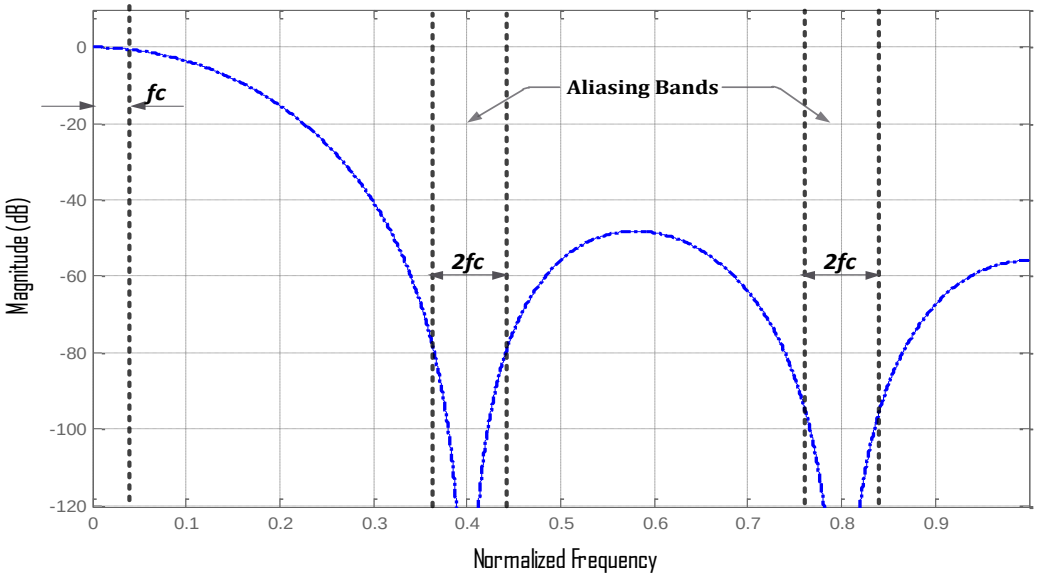


Figure III-25 Transfer Function of Decimation Filter with N=4, M=1, and R=5

III.12 Digital Baseband Processing

The digital baseband transmitter is responsible for loading the binary data onto a carrier or multiple carriers under known format. At the baseband receiver, data is unloaded from the carrier, in other words baseband module is responsible for modulation and demodulation of the data that is being transmitted.

Figure III-26 shows the modules of the baseband transceiver, by using different modulation and coding schemes, the user's data bits are coded into samples by the trellis/convolutional coding. Those samples are then mapped into complex baseband signal with different modulation (e.g., BPSK, QPSK, 16-QAM, 8-PSK etc.).

An optional frequency/time division multiplexing is then applied to generate a multi-carriers/multi-users transmission scheme. These include single-carrier (SC), orthogonal frequency-division multiplexing (OFDM), and code division multiple

access (CDMA) etc. The last optional stage is the digital pre-distortion. The Pre-distortion function is applied to compensate for different impairments that are related to the RF frontend. The power amplifier's nonlinearity is the most important constraint that should be compensated at the transmitter.

At the receiver, the baseband module processes the baseband signal and extracts the data. At the first stage, and in order to cancel multipath propagation, equalization is performed to mitigate the inter-symbol interference (ISI) due to the frequency selective response of the channel. For any multiplexing functions performed at the transmitter, a de-multiplexing should be applied at the receiver to recover the original baseband signal.

Respective to the modulation employed, the equalized and de-multiplexed baseband signal is then de-mapped and demodulated through trellis or Viterbi decoder to deliver the originally transmitted bits.

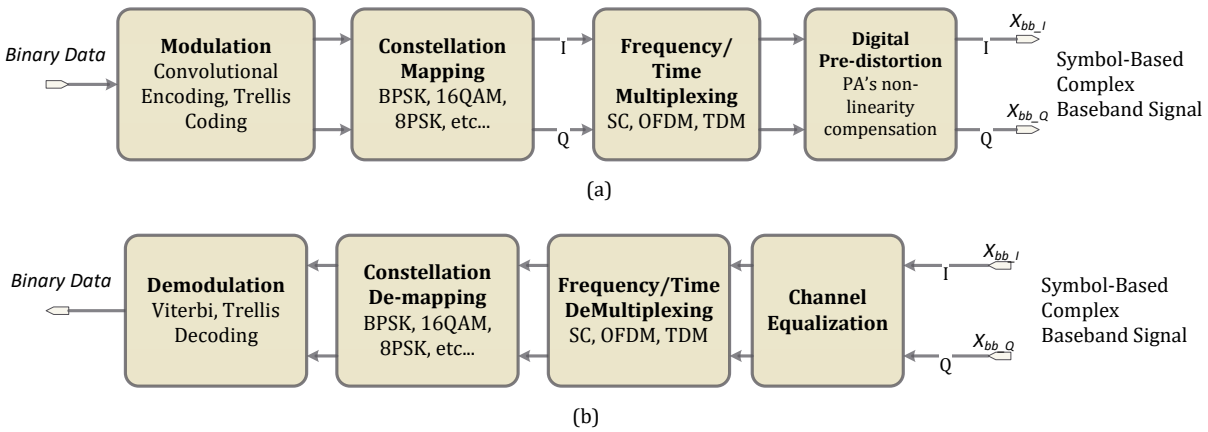


Figure III-26 Baseband Modules of Transmitter (a) and Receiver (b)

III.13 Data Conditioning

Usually considered as the digital backend of the transmission chain, this processes the raw user's data before transmission. As shown in Figure III-27, data conditioning includes forward error control (FEC) where redundant bits are added to the raw data. Reed-Solomon (RS), low-density parity-check (LDPC) and/or Convolutional/Viterbi coding schemes are employed along with interleaving/de-interleaving mechanisms to enhance the FEC capabilities. In addition, framing, bits-stuffing, and data-encryption occur in the digital backend. Respective to the coding schemes employed at the transmitter, the receiver's backend performs decoding operations to extract the transmitted user's data [23].

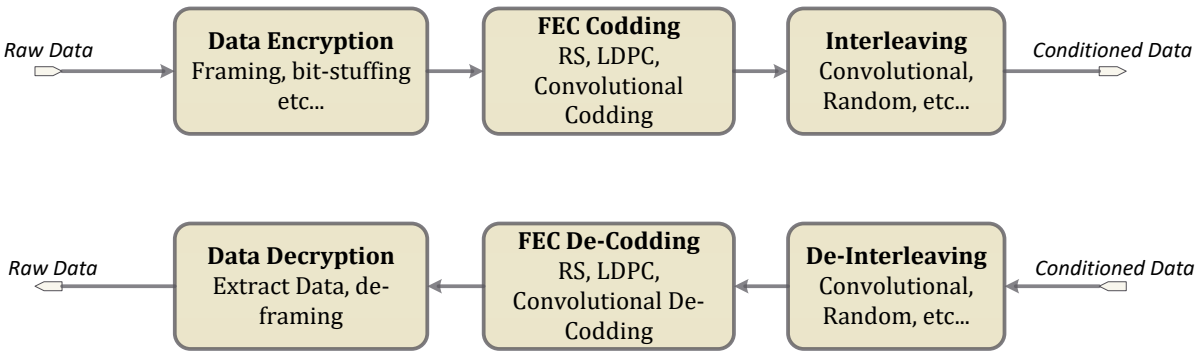


Figure III-27 Data Conditioning Digital-Backend

III.14 SDR Enabling Technologies

Three main categories of digital hardware technologies are considered in software-defined radio implementations. These are: application specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), and digital signal processors (DSPs)[31].

III.14.1 Application-Specific Integrated Circuits (ASICs)

Beginning in the 1980s, the application-specific integrated circuit (ASIC) is an integrated circuit that is customized for specific applications. Digital, analogue, or mixed micro-circuits that carry out basic functions (i.e., amplification, ADC/DAC conversions, digital filtering etc.) are combined to perform a special purpose. The highly optimized implementations of those circuits on fixed-silicon, results an optimized integrated circuit (IC) in terms of speed and power consumption.

III.14.2 Field Programmable Gate Arrays (FPGAs)

The field programmable gate array (FPGA) was first introduced by Xilinx in mid-1985s. An FPGA is an integrated circuit that contains a large array of identical logic cells with programmable interconnects. Cells can be grouped into logic blocks to form higher-level functions (e.g., lookup tables, multiplexers, adders, multipliers, and RAM memories).

III.14.3 Digital Signal Processors (DSPs)

The digital signal processor (DSP) was first introduced in the early 1980s in order to provide micro-processors that are optimized for interpreting, manipulating, and generating digital signals in the time or frequency domain. The DSPs include special instructions in the microcode optimized for signal processing. These include multiply and accumulate (MAC) operations which are highly involved in FIR filters and

convolutions. The program control flow features accelerate common DSP tasks such as FFT or Viterbi decoding.

As shown in Figure III-28, those technologies provide tradeoffs between flexibility (functions capability) and performance (speed and power consumption) at which those functions run [31, 41] :

Flexibility: the flexibility refers to the ability of a device to handle a variety of digital signal processing functions, and how likely those functions may have to be changed or customized for any specific application. Tasks that are based on analysis and decision with software implementation, like demodulation, and forward error control, DSPs are usually chosen for the implementation of those tasks.

Performance: the device performance can be quantified by the speed at which the signal processing functions are executed, the consumed power, and relative cost. Functions like digital up/down-conversions, and signal filtering, those functions require highly pipelined multiplications functions that require specialized hardware structures in order to achieve a real-time signal processing, hardwired devices such as ASICs are usually the norm to implement this kind of functions.

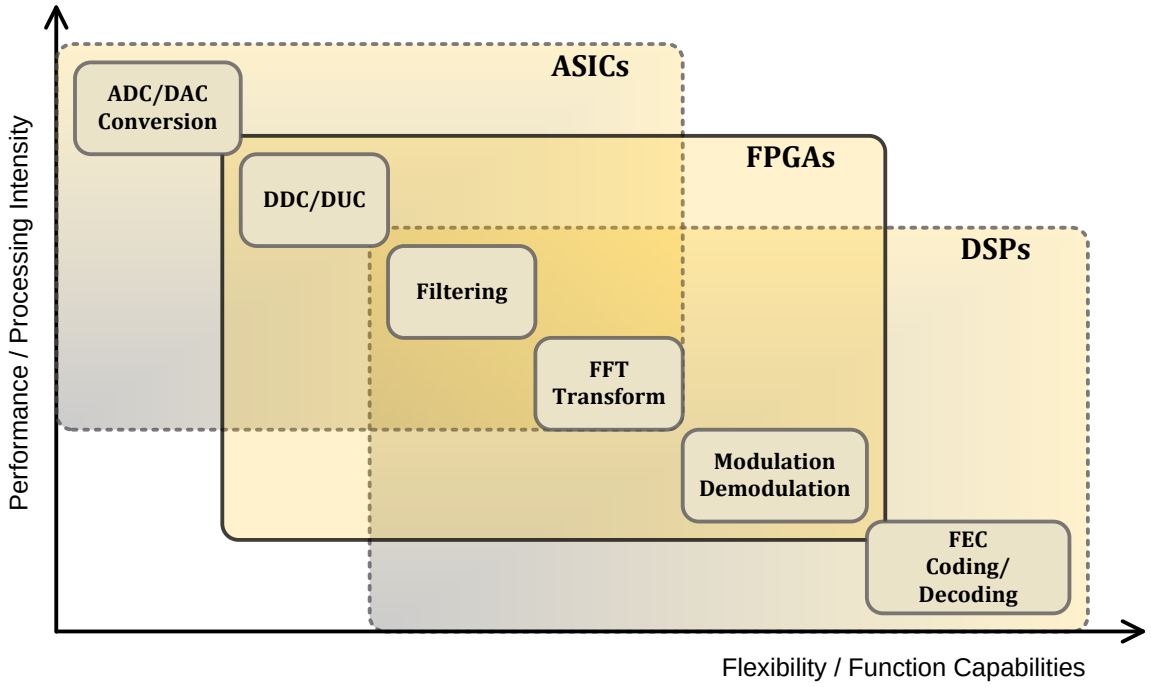


Figure III-28 Performance vs. Flexibility of Digital Hardware Technologies

Figure III-28 illustrates how the FPGA can provide the best solution for software-defined radio system, where both high performance (vital in the digital up and down conversions, filtering) and a high degree of software functions flexibility (required in the demodulation and decoding) are guaranteed.

Furthermore, the latest generations of FPGAs are not just a massive array of inter-connectable gates, but contain dedicated general-purpose processor cores, random access memories (RAMs) and embedded multipliers to perform arithmetic operations that would be required in the software-defined radios. FPGAs greatly relax the processing architecture constraints and enable custom processing architectures while keeping the flexibility of processor software [42]. Recent FPGAs offer the advantages of parallel hardware to handle high process-intensity functions and the benefit of software programmability to accommodate some of the decoding and analysis functions of DSPs [41].

III.14.4 FPGA Design Tools

To support the recent advances and complexity in the FPGA devices, there has been considerable progress in software design tools to support DSP applications on FPGAs. Many FPGAs and tools manufacturer have developed high-level development tools, where the complexity of the FPGA chip is totally abstracted, by using high-level language such as C, C++ or Java instead of hardware description languages HDLs. Furthermore, and in order to develop an efficient and less time-consuming development methodologies for digital signal processing applications, big FPGA manufacturers such as Altera with its “DSP Builder”, and Xilinx with its “System Generator”, have developed tools for DSP design based on Matlab/Simulink [43].

System Generator is a DSP design tool from Xilinx that enables the use of the Mathworks Simulink model-based design environment for FPGA design. System Generator abstracts the low-level hardware description language (e.g., VHDL, or Verilog) by providing graphical functional modules; using system generator does not require a deep knowledge of such complex languages [44].

Similar to Matlab Simulink blockset, system generator blockset are used to build a sophisticated DSP system with bit and cycle accurate modelling and simulation. Bit-accurate blocks produce values and precisions in Simulink that match the

corresponding values and precisions produced in hardware; cycle-accurate blocks produce corresponding values at the corresponding hardware clock's cycles. Figure III-29 shows a sample of those blocks, mathematical, logic, DSP, and memory manipulation functional blocks are provided [45].

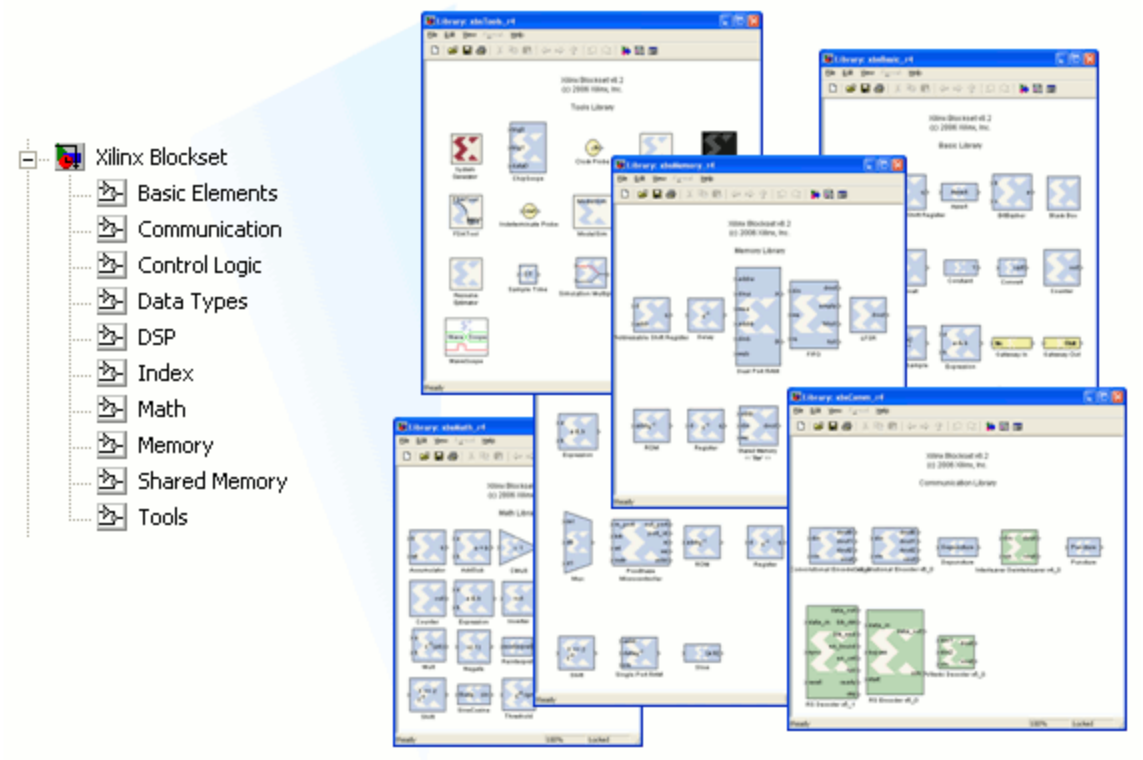


Figure III-29 Snapshot of System Generator Blockset

In addition of the elementary blocks, a large number of predefined and highly optimized cores are available to implement system-level design. This enables customers to reduce development time, design risk, and get access to the best performance for their designs. These Intellectual Property (IP) cores available from Xilinx and third-party partners are commonly used to perform complex functions such as DSP, bus interfaces, microprocessors, and processor peripherals [46].

As shown in Figure III-30, in System Generator, the design starts by either fixed-point, floating point or even mixed types simulation and validation using Simulink as modelling interface. Once the design is verified and validated, System Generator automatically compiles the system design into efficient low-level hardware description language (VHDL/Verilog) along with the integration of the employed IP cores. Those tasks are performed by the Xilinx integrated software environment (ISE) that is running in the background when implementing System Generator blocks. The

generated files are then synthesized, placed and routed into a physical file that can be downloaded on the target FPGA.

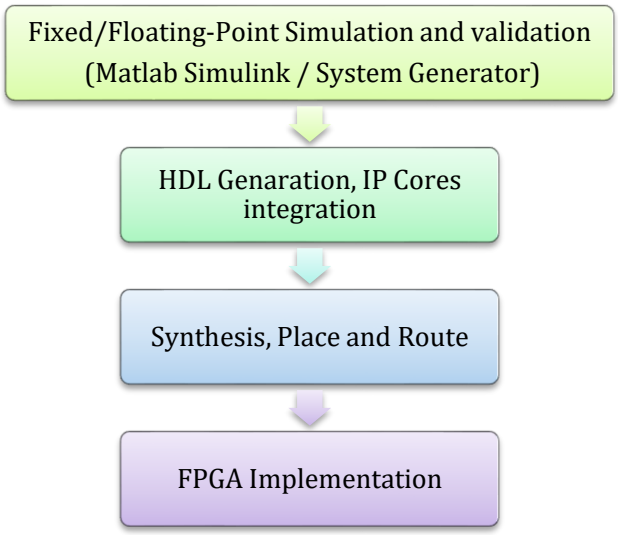


Figure III-30 System Generator Design Flow

III.15 Platforms for Software-Defined Radio

Software-defined radio (SDR) research has been primarily motivated by interoperability problems between different radio standards and air interfaces, that result from the implementation of radio systems in dedicated hardware [23].

A majority of software-defined radio implementations that exist are often achieving a small bandwidth (dozens of MHz), that makes them capable to achieve only low data-rate (dozens of Mb/s). Thus, no millimetre-wave SDR platform exists capable to achieve multi-Gb/s data-rate over the 60 GHz frequency band. Table III.1 illustrates most of the available SDR platforms.

III.15.1 Universal Software Radio Peripheral (USRP)

The USRP is one of the most popular SDR platforms currently available, and produced by Ettus Research. A typical USRP platform consists of a motherboard with high speed digital signal processing Xilinx Spartan-III FPGA, and one or more daughter boards contain the RF frontends to cover different frequencies range. All daughter boards family covers from DC to 5.9 GHz, with around 25 MHz of bandwidth [47].

The USRP and GNU Radio, provide to engineers and designers a powerful combination of flexible hardware, with an open source runtime library and functional blocks to implement software radios. The GNU Radio is a free, open-source software

development kit that provides digital signal processing runtime library to build a software radios. It is widely used in hobbyist, academic and commercial environments to support both wireless communications research and real-world radio systems. GNU Radio is primarily written using the Python programming language, while performance-critical signal processing paths are implemented in C++. Thus, the developer is able to implement real-time, high-throughput radio systems in a simple-to-use, rapid-application-development environment [48].

III.15.2 Kansas University Agile Radio (KUAR)

The KUAR platform is a low-cost experimental platform that targets the frequency range 5.25 to 5.85 GHz and a tuneable bandwidth of 30 MHz. The KUAR includes an embedded 1.4 GHz general purpose processor (GPP), a Xilinx Virtex-II FPGA and supports gigabit Ethernet and PCI-Express bus connectivity to the host PC Computer. This allows almost all the signal processing functions to be implemented on the platform and minimize the host-interface communications requirements. The KUAR employs a modified version of the GNU Radio software development framework to programme the hardware platform [49].

III.15.3 Berkeley Cognitive Radio Platform (BWRC-BEE2)

This platform provides a testbed to experiment indoor cognitive radios with sensing algorithms. The BWRC SDR platform is based on Berkeley emulation engine (BEE2) which is a FPGA based emulation platform for computationally intensive applications that contains 5 high-powered Virtex-II FPGAs and capable of connecting to 18 RF daughter boards. The radio daughter boards support up to 25 MHz of bandwidth within 85 MHz sensing range in the 2.4 GHz ISM Band. The BEE2 platform can be programmed using Matlab/Simulink coupled with the Xilinx system generator and a set of parameterized library blocks [50].

III.15.4 NICT SDR Platform

This SDR platform was designed by the Japanese national institute of information and communications technology (NICT) to experiment next generation mobile networks. The platform made around two embedded processors, 4 Xilinx Virtex-II FPGAs for digital signal processing, and RF daughter board to support 1.9 to 2.4 and 5.0 to 5.3 GHz frequency band. The main aim of this platform was to explore selection of algorithms and manage handover between existing commercial standards, for

example, 802.11a/b/g, digital terrestrial broadcasting (Japanese format), WCDMA, and a general OFDM communication scheme [51].

Table III.1 Some of the Available SDR Platforms

	USRP	**KUAR**	**BWRC-BEE2**	**NICT**
Year of release	2008	2005	2007	2005
RF bandwidth (MHz)	25	30	25	25
Frequency range (GHz)	2.3-2.9	1.7-2.5	Fixed (2.45)	1.9-2.4
Processor architecture	GPP/FPGA	GPP/FPGA	FPGA	GPP/FPGA
Connectivity	USB	USB/Ethernet	USB/Ethernet	USB/Ethernet
No. of antennas	2	2	16	2

III.16 Conclusion

In this chapter, the concept of software-defined radio (SDR) with its architecture has been introduced. An overview of the functional architecture of the SDR has been described and digital solutions to implement those modules were discussed.

Considered as fundamental process in SDR, the sampling theorem and analogue signal digitization were deeply analysed. Thus, the features of the ADCs converters, which are key components in the SDR receiver, were characterized. It has also been discussed that recent FPGA technologies offer great digital signal processing capabilities to implement SDR radios, while keeping the performance of an ASIC and the flexibility of a DSP processor required in the SDR.

CHAPTER IV
FPGA Implementation OF BASEBAND SC-FDE AND OFDM COMMUNICATION SCHEMES

IV.1 Introduction

This chapter details the design and implementation of the baseband components that made the proposed millimetre-wave transceiver, two transmission modes are considered: the orthogonal frequency-division multiplexing (OFDM) and single-carrier with frequency domain equalization (SC-FDE). Taking into consideration the IEEE 802.15.3c physical (PHY) layer [2], basically, the two modes employ common functional blocks as demonstrated in CHAPTER II.

IV.2 16-QAM SC-FDE/OFDM Baseband Transceiver

Figure IV-1 shows the block-diagram of the implemented SC-FDE/OFDM transceiver. At the transmitter, a data source is employed to generate pseudo random bits which are coded with forward error control (FEC) block then mapped into complex symbols using 16-QAM modulation scheme with constellation shown in Figure IV-2. In OFDM mode, the modulated symbols are mapped into N subcarriers through N-Points FFT transform, whereas, in SC-FDE mode the symbols are modulated to one carrier. Next, a guard interval (GI=32) is inserted between data sub-block then synchronization (SYNC), start frame delimiter (SFD), and channel estimation sequences (CES) are prefixed at the beginning of the data sub-blocks as defined in the IEEE 802.15.3c standard. In this system and for maximum spectrum efficiency only four samples per symbol (up-sampling factor equals to four) are used. The up-sampled signal is then shaped by a root-raised-cosine (RRC) filter to limit the bandwidth of the transmitted signal and hence avoid inter-symbol interference (ISI). To compensate for the IQ imbalances of the IQ Mixers at the RF frontend, an IQ pre-distortion is applied before that the signal is converted to analogue signal prior to transmission.

At the receiver, the received baseband signal is converted to digital format through an ADC operating from a clock source that is identical to that employed in the DAC at the transmitter. At the first stage, a DC-Canceller removes any DC components caused by the ADC converter or the RF frontend receiver. The digital samples are then shaped

using the RRC filter similar to that employed in the transmitter to reduce out-of-band frequency, noise, and spectrum images. Next, carrier recovery (CR) and an automatic gain control (AGC) are then performed in order to provide a sufficient signal level with a correct phase to the following stages.

For equalization purpose, the channel impulse response is estimated through the cross-correlation of the known channel estimation training sequences (CES). The correlation of the SYNC and SFD training sequences is also performed, in order to tag the starting positions of the channel impulse responses and data sub-blocks that is mandatory to perform the FFT over a precise window. After the FFT of the impulse response frame is completed, the equalization of the data's spectrum is performed with the aid of estimated channel frequency response. In SC-FDE mode the equalized signal is then transformed to time domain by applying inverse Fourier transform (IFFT) prior to the 16-QAM demodulation and FEC decoding is used to recover the transmitted data. However, in OFDM signal the subcarriers are demodulated in frequency domain, therefore, no IFFT transform is used.

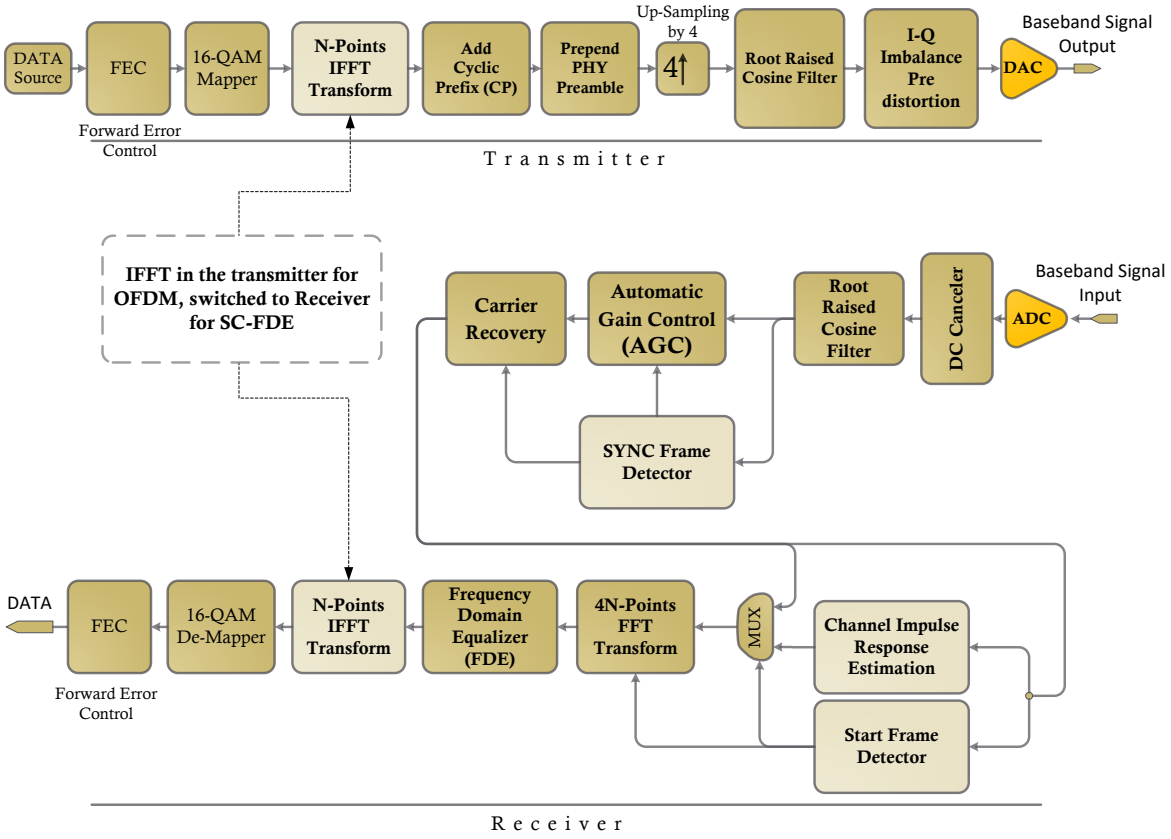


Figure IV-1 The Implemented SC-FDE/OFDM Baseband Block-Diagram

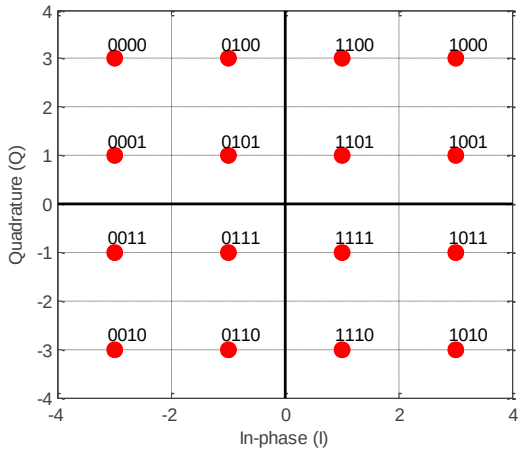


Figure IV-2 Constellation of 16-QAM Quadrature Modulation

IV.2.1 Golay Sequence Based Preamble for SC-FDE/OFDM

Recently, Golay complementary sequences have been proposed in the third cellular and wireless local/personal area networks (WLANs/WPANs), for use in the preamble for synchronization and channel estimation. Golay sequences have been widely used to detect a signal immersed in noise. A pair of Golay sequences (a_N, b_N) have an attractive property that the addition of their a-periodic auto-correlation functions equals to zero for all nonzero time shifts, in other words, the sum of their auto-correlations has maximum peak and no side-lobes [52]. Let [a_N, b_N] be the pair of complementary Golay sequences of length equals to $N=2^M$ (M natural number) and [R_a, R_b] the auto-correlation of a_N and b_N respectively. The Golay sequences are defined by the following auto-correlation property:

$$\mathrm{R_{ab}}(i) = R_a(i) + R_b(i) = 2\mathrm{N}\delta(i - N) \qquad \text{Eq. IV.1}$$

Where $\delta_{(i)}$ is the Kronecker delta function.

Golay sequences have not only excellent autocorrelation property, but also a low complexity correlator. An efficient matched filter directly related to the sequences {a_N, b_N} is given in Figure IV-3. This matched filter performs simultaneously the correlation of the input signal $x_{(k)}$ with the two complementary sequences {a_N, b_N}, the two corresponding outputs produce the two a-periodic correlation functions {R_a, R_b}. Such digital matched filter is called an efficient Golay correlator (EGC) [52]. For binary Golay sequences of length 2M, the number of multiplications and additions equal to $\log_2$ M and 2×$\log_2$ M respectively, while in straightforward matched filter implementation it would be M and M-1 respectively [53].

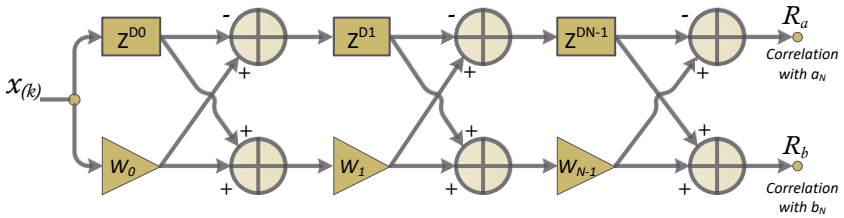


Figure IV-3 Efficient Golay Correlator (EGC)

Figure IV-4 shows the IEEE 802.15.3c proposed physical (PHY) frame [53], which consists of a preamble, a header, and a packet payload. The preamble consists of packet synchronization sequence (SYNC), a start of frame delimiter (SFD), and a channel estimation (CE) sequence fields. The packet payload consists of data frames separated by a guard interval (GI), which could be treated as the cyclic prefix in OFDM systems. Each sub-block is considered as one FFT window. The inter-block interference introduced by the time-dispersive channel can be eliminated, as long as the length of the guard interval is greater than the wireless channel delay. The guard interval can be filled with a known sequence in order to facilitate the coarse frame timing and carrier frequency recovery or kept blank. The frame header conveys information about the PHY and MAC (i.e., modulation schemes, coding, and spreading factor etc.) of the current transmission. The header part is not employed in this design since only 16-QAM modulation is adopted [7].

The synchronization (SYNC) part is used to aid the receiver's algorithms related to automatic gain control, timing and carrier frequency recovery. For channel complex impulse response (CIR) estimation, the channel estimation sequences (CES) contains Golay complementary sequences (a_N, b_N) of length equals to 128. The a_N and b_N sequences are repeated M times in order to realize M channel impulse responses, and then averaged to reduce the noise effect. Each pattern is preceded by a cyclic prefix (a_{pre}, b_{pre}), copy of the last half of the sequence, and followed by a cyclic postfix (a_{pos}, b_{pos}), copy of the first half of the sequence.

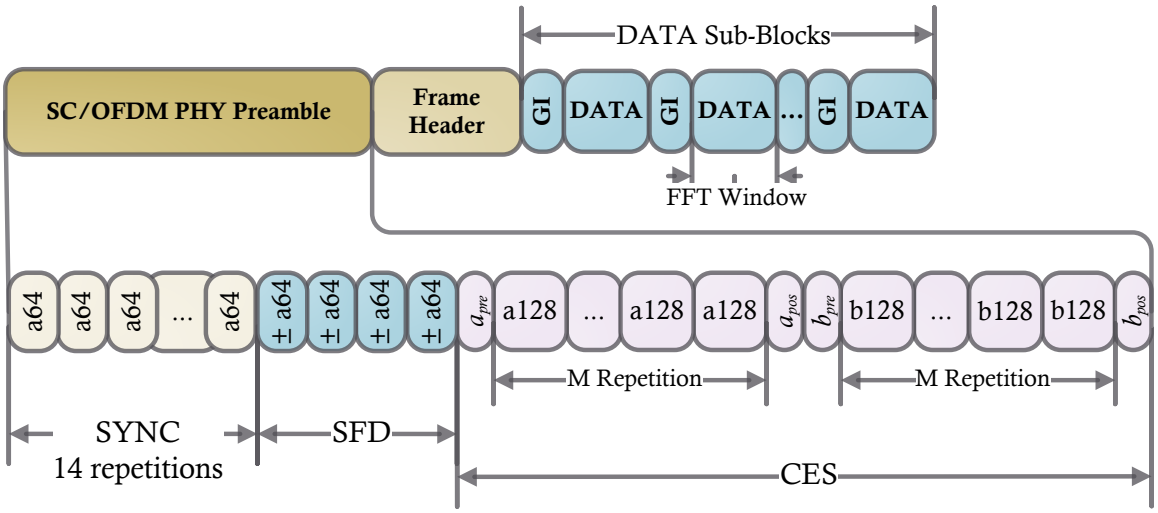


Figure IV-4 Frame Format for SC-FDE/OFDM Transmission Modes

IV.2.2 Golay Sequence Aided Channel Estimation

Considering the adopted channel estimation sequence (CES) preamble of Figure IV-5, the CES consists of two parts (a_{ces} and b_{ces}), with both have common configuration of M repetitions of complementary sequences A128 and B128 with the base sequence length N_{ces} equals to 128, prefix and postfix sequences which are the last and first half of the base sequences (a128, b128) respectively, inserted at the head and the end of each repetition.

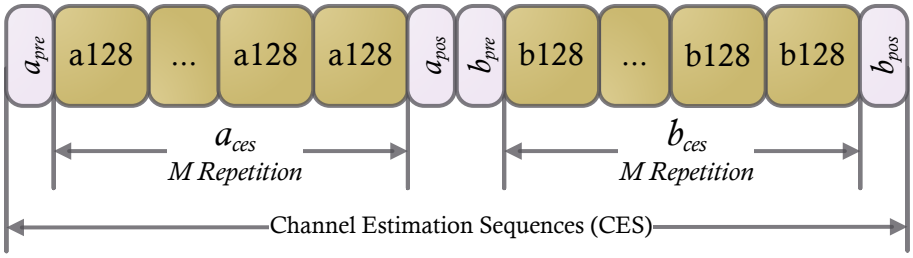


Figure IV-5 Channel Estimation Sequences (CES) Employed for Impulse Response Estimation

At the receiver, the received CES sequences, after passing through a channel with impulse response $h_{(k)}$, are expressed as:

$$r_{ces(n)} = \sum_{k} h_{(k)} CES_{(n-k)} \qquad \text{Eq. IV.2}$$

The Golay correlator calculates the correlation between the received CES sequences and the respective Golay complementary sequences (a_{NCE}, b_{NCE}) as follows:

$$r_{a(n)} = \frac{1}{N_{CES}} \sum_{k=0}^{N_{CES}-1} r_{ces(n-k-N_{CES}+1)}\, a^*_{NCE(k)} \qquad \text{Eq. IV.3}$$

$$r_{b(n)} = \frac{1}{N_{CES}} \sum_{k=0}^{N_{CES}-1} r_{ces(n-k-N_{CES}+1)}\, b^*_{NCE(k)} \qquad \text{Eq. IV.4}$$

Aligning the two correlations and discarding postfix and prefix, the sum of the two correlation functions provides the channel impulse response $\hat{h}_{(n)}$ at the m^{th} sequence:

$$\hat{h}_{(m,n)} = \frac{1}{2} \sum_{m=0}^{M-1} r_{a(n+mN_{CES})} + r_{b(n+mN_{CES}+(M+\frac{3}{2})N_{CES})} \qquad \text{Eq. IV.5}$$

Figure IV-6 shows the two EGC correlators employed to generate a complex impulse response (CIR). As long the received signal is not decimated (originally up-sampled by four), this factor is taken into consideration when designing the EGC by multiplying all delays by this factor. The generated M channel impulse responses are shown in Figure IV-7.

Using the discrete Fourier transform over $4N_{CES}$ points, the m^{th} channel complex frequency response (CFR) at the n^{th} frequency component can be written as:

$$\hat{H}_{(m,n)} = \mathrm{DFT}\{\hat{h}_{(m,n)}\} = \frac{1}{4N_{CES}} \sum_{k=0}^{4N_{CES}-1} \hat{h}_{(m,k)}\, e^{-j\left(\frac{2\pi k}{4N_{CES}}\right)n} \qquad \text{Eq. IV.6}$$

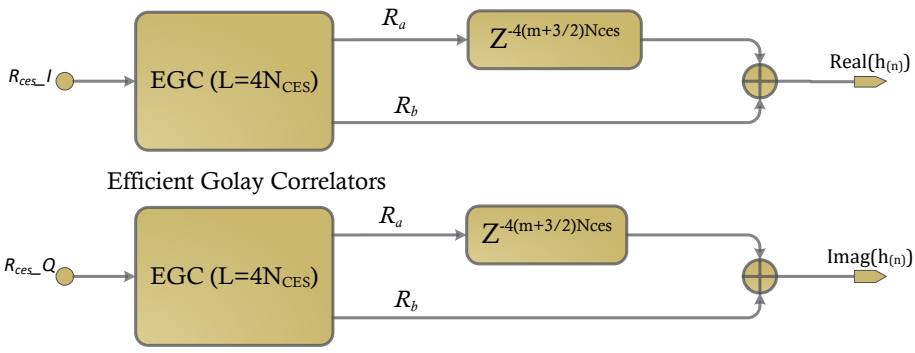


Figure IV-6 CES Correlator to Generate Channel Impulse Response $h_{(n)}$

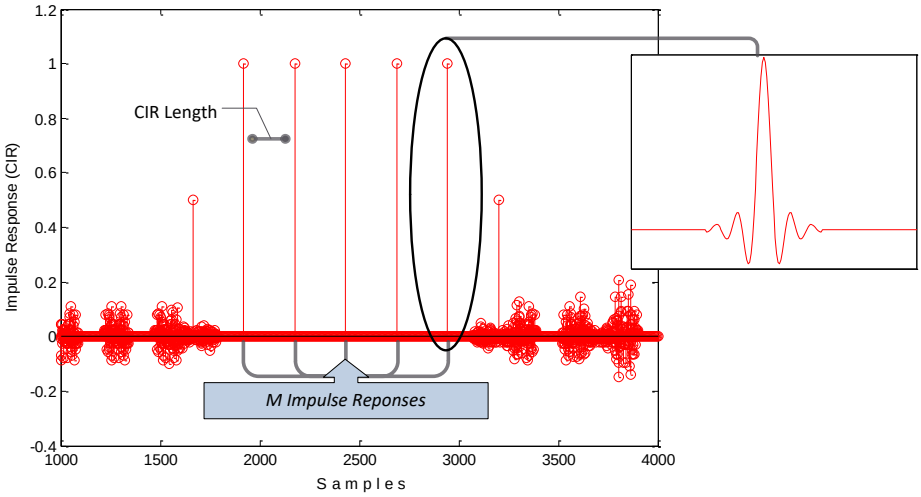


Figure IV-7 Channel Impulse Response Generated By the Correlation of the M CES Sequences

IV.2.3 Fractionally-Spaced MMSE Frequency Domain Equalization

Once the channel frequency response (CFR) estimated, a straight forward compensation of any channel frequency selective fading in the spectrum of the transmitted signal is achieved, by simply multiplying the received spectrum by the inverted CFR, ($w_{(n)}^{ZF} = \frac{H_{(n)}^{*}}{|H_{(n)}|^2}$). However, this may result in noise enhancement in the frequency components that undergo a deep fading, especially in multi-Gb/s wireless transmission where deep fading occurs frequently. In the minimum mean square error (MMSE) equalizer, which tries to minimize the resulting noise, the equalization weights $w_{(n)}^{MMSE}$ are estimated as follows [54]:

$$w_{(n)}^{MMSE} = \frac{\hat{H}_{(n)}^{*}}{\left|\hat{H}_{(n)}\right|^2 + \frac{\sigma_{noise}^2}{\sigma_{signal}^2}} \qquad \text{Eq. IV.7}$$

Where σ_{signal}^2 and σ_{noise}^2 are the signal and noise power respectively, estimated as follows:

$$\sigma_{signal}^2 = \frac{1}{N}\sum_{n=0}^{N-1}\left|\hat{H}_{(n)}\right|^2 \qquad \text{Eq. IV.8}$$

$$\sigma_{noise}^2 = \frac{1}{MN}\sum_{m=0}^{M-1}\sum_{n=0}^{N-1}\left|\hat{H}_{(n)} - \hat{H}_{(m,n)}\right|^2 \qquad \text{Eq. IV.9}$$

Where $\hat{H}_{(m,n)}$ is the channel frequency response at the m^{th} CES sequence and $\hat{H}_{(n)}$ the averaged channel frequency responses over M sequences.

At the end, the phase and the amplitude of the n^{th} data subcarrier $X_{(n)}$ can be equalized by single-tap equalization using the n^{th} MMSE coefficient $w_{(n)}^{MMSE}$:

$$Y_{(n)} = X_{(n)} \times w_{(n)}^{MMSE} \qquad \text{Eq. IV.10}$$

The fractionally-spaced equalizer technique is adopted in this design in order to eliminate the timing recovery circuitry. In this case a 4N-Point FFT transform is applied on the received samples, originally up-sampled by the factor of four at the transmitter. This leads to transferring the sampling error (timing offset) to the frequency domain and appears as a phase offset on the spectrum. This allows a frequency domain equalization and timing recovery to be performed simultaneously [55].

Figure IV-8 illustrates the implemented fractionally-spaced MMSE equalization. Following the estimation of the channel impulse response $\hat{h}_{(m,n)}$, as described in section IV.2.2, 4N point FFT transform is performed to estimate the channel frequency responses (CFRs) $\hat{H}_{(m,n)}$. The output of this FFT consists of 4 replicas of the original CFR, hence, a FIFO is employed to get rid of these replicas and down sampling the signal by a factor of 4. After that, the signal-to-noise ratio (SNR), estimated by employing equations Eq. IV.8 and Eq. IV.9, and implemented as shown in Figure IV-9. The estimated SNR is then employed to calculate the MMSE weights using equation Eq. IV.7, those weights are then used to equalize the data's spectrum as described in Eq. IV.10.

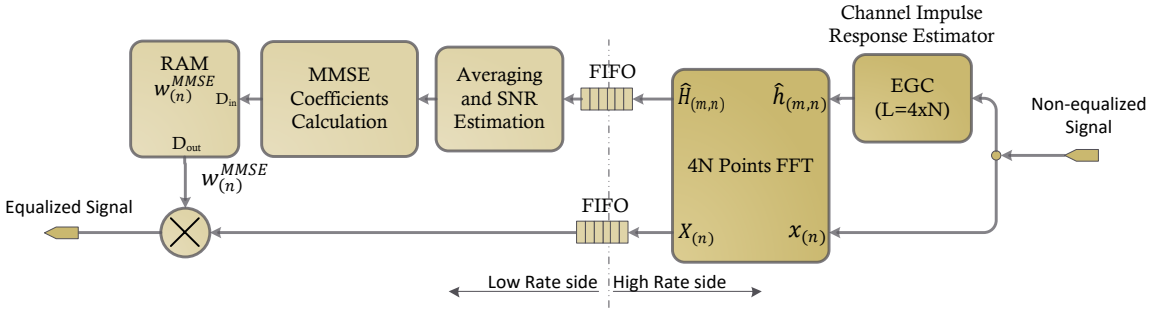


Figure IV-8 Block Diagram of the Fractionally-Spaced MMSE Equalizer

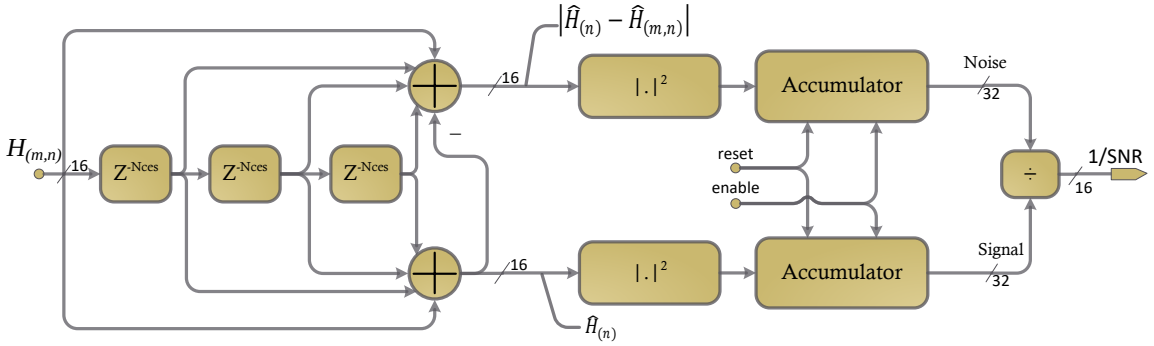


Figure IV-9 Block Diagram of the Signal-to-Noise Ratio Estimator

IV.2.4 SYNC and SFD Frames Detector

The SYNC sequences, as described in section IV.2.1, help to perform the automatic gain control (AGC) and carrier recovery (CR), hence, the detection of this preamble is mandatory to activate the automatic gain control (AGC) and carrier recovery (CR) during the reception of the SYNC sequences.

Figure IV-10 illustrates the block diagram of implemented SYNC frame detector. It detects the 'a64' Golay sequences that make the SYNC. Thus, an efficient Golay correlator (EGC) matched with the respective sequences is used. The normalized EGC's output R_a is then auto-correlated with its delayed copy by 64×4 samples, which take into consideration the up-sampling factor. The correlation output contains positive peaks that tag the occurrence of the SYNC sequences. Figure IV-11 shows the EGC's output and the correlated signal, which is compared to a positive threshold to make a decision about the presence of the SYNC. Simulation results of the miss and false detection probabilities for Signal-to-Noise Ratio of 0 dB are shown in Figure IV-12. Using a high threshold the detection of the preamble can be missed; whereas, a low threshold leads to false alarms. The optimal value of the threshold is located between the two graphs, where miss and false detection probability are minimal.

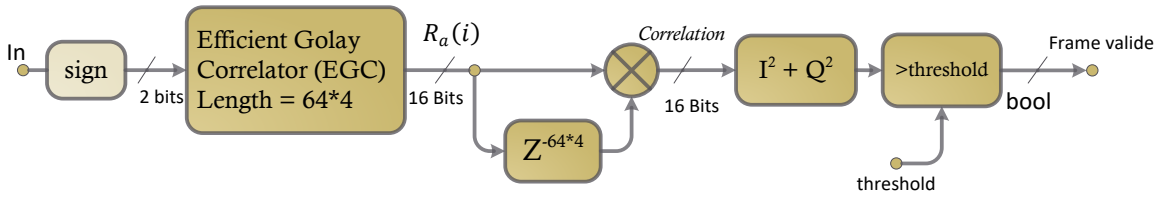


Figure IV-10 Block Diagram Schematic of the SYNC Frame Detector

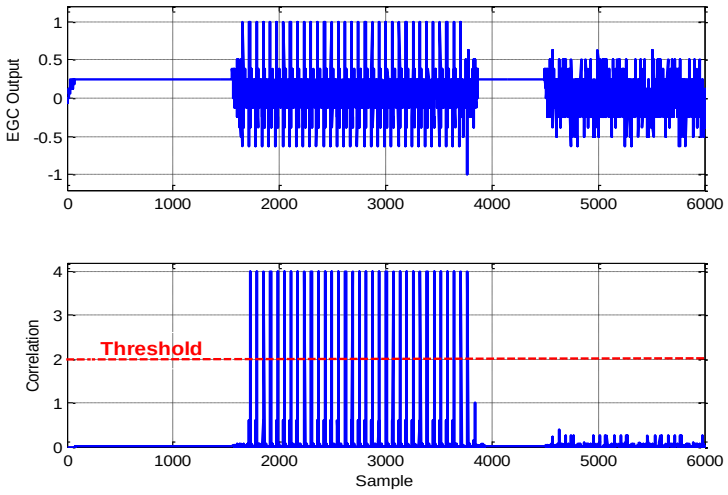


Figure IV-11 Output of the EGC (R_a) and its Autocorrelation

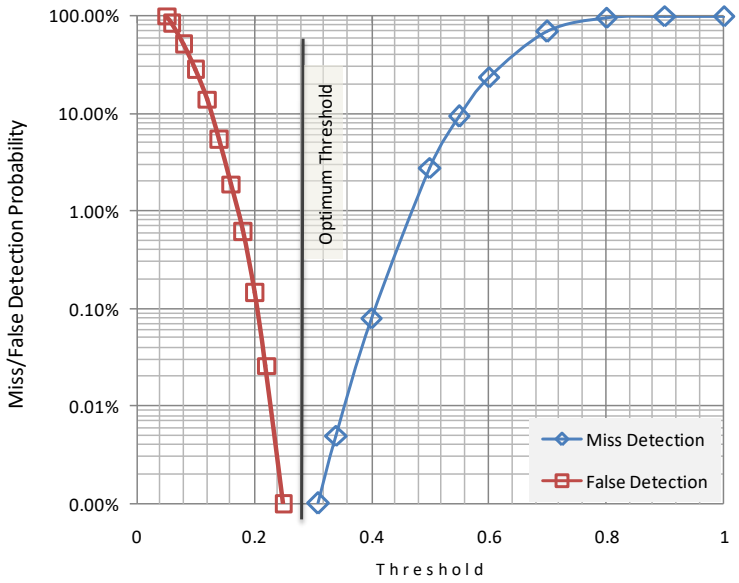


Figure IV-12 Probability of Miss and False Detection versus Normalized Threshold at SNR = 0 dB

To perform the FFT transform over an exact window in both SC-FDE and OFDM, the start frame delimiter (SFD) of the preamble shown in Figure IV-4 helps to mark the start positions of CES sequences and the data sub-blocks in order to perform the FFT transform over a precise window.

Figure IV-13 shows the schematic of the correlator employed to detect both the positive peaks that tag the SYNC sequences and negative peak relative to the last sequence of the CFD part that consists of [A64 A64 A64 -A64]. The decision is made when a certain number of positive peaks detected followed by a negative peak.

Once the negative peak is detected, a state machine triggers the FFT transform at the start positions of CES sequences and data sub-blocks as long the metric distances between SFD, CES, and data are known.

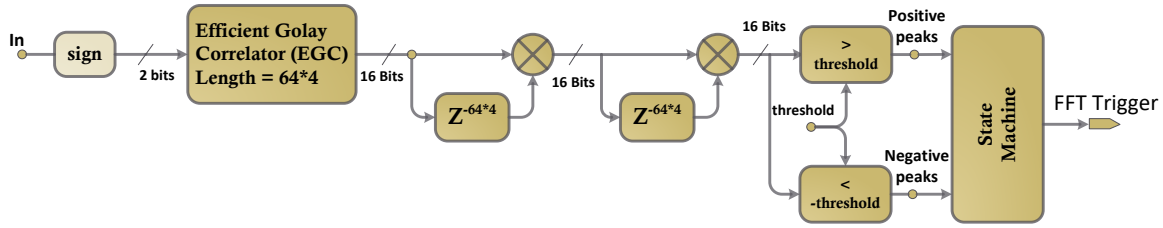


Figure IV-13 Block Diagram of the Start Frame SFD Detector

IV.2.5 Automatic Gain Control (AGC)

In the receiver, the received signal has an unpredictable power level and varies over a wide dynamic range due to both large and small scale multipath fading. Therefore, an automatic gain control (AGC) loop is necessary for dynamically adjusting the power of the incoming signal to minimize the computation error and prevent the overflow/underflow in the subsequent digital signal processing modules [56].

Basically, AGCs can be implemented in two structures: feed-forward and feed-backward. In feed-forward AGC, the input voltage controls the output voltage by continuously adjusting the output gain to keep a constant output. Feed-forward (i.e., open loop) AGC has the advantage to be intrinsically stable because it does not incorporate feedback. In the feed-backward structure (i.e., closed loop), the estimated output voltage is compared with a reference to generate an error signal, this error is sent to adjust the input signal until the error is cancelled, The loop filter guarantees the stability of the feedback loop, and precautions should be taken to avoid instability. For the sake of stable AGC mechanism the feed-forward is adopted in this design, Figure IV-14 shows the proposed schematic of feed-forward AGC, to avoid the square-root and multiplication functions (i.e., functions requiring important FPGA resources), an approximation is used to estimate the module of the input voltage, as follows:

$$V_{est} = \sqrt{I^2 + Q^2} \approx |I| + |Q| \qquad \text{Eq. IV.11}$$

The absolute value function can be realized with a multiplexer (MUX), where sign bit of the input switches the MUX between the two inputs –I and +I. The estimated voltage is then smoothed to reduce noise and glitches. The smooth function is realised with a moving average over 64 samples (more samples are used more the signal is smooth). To adjust the output voltage, a fixed reference value V_{ref} is divided by the estimated input voltage to generate a gain value that locks the output voltage around the fixed reference V_{ref}. To perform the division, the Xilinx IP-core that implements a coordinate rotational digital computer (CORDIC) algorithm is employed. The division is enabled only during reception of the SYNC part of the preamble, to make the input voltage estimation more accurate due to the constant envelop of the SYNC sequence.

The dynamic range (DR) is directly related to the number of bits used in the division (B) as follows:

$$DR_{dB} = 10\log_{10} 2^{B-1} = 3(B-1) \qquad \text{Eq. IV.12}$$

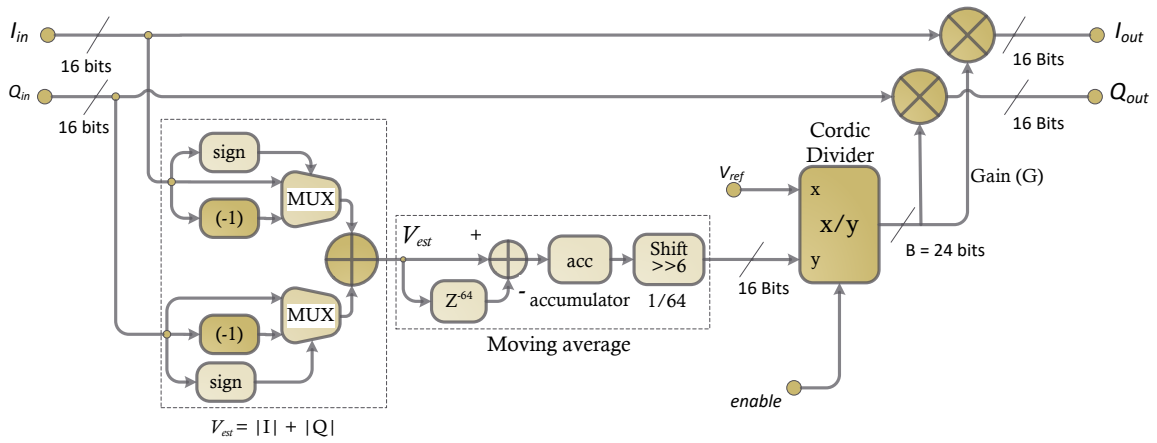


Figure IV-14 Schematic Block Diagram of the Implemented Feed-Forward AGC

IV.2.6 Carrier Frequency Recovery

In both SC-FDE and OFDM, a carrier frequency offset error exists due to the mismatch between the local oscillators of transmitter and receiver. In OFDM, the frequency offset results in inter-carrier interference, which destroys the orthogonality among the subcarriers, whereas, in SC-FDE frequency offset corrupts the modulated phase of the received signal. Therefore, accurate frequency synchronization is needed to recover the correct carrier frequency.

Exploring the periodic property of the SYNC preamble of the Figure IV-4, which contains 14 repetitions of 'A64' sequences, the carrier frequency offset (CFO) information is embedded in each cross-correlation between two consecutive 'A64' sequences [57]. Hence, considering CFO equals to ΔF, and sampling rate T_s, the cross-correlation between the received signal (r_k) and its L-samples shifted copy (r_{k-L}), with L = 64, length of the 'A64' Golay sequence, is written as follows:

$$Y_n = \sum_{k=0}^{L-1} r_{n-k}^{*} \times r_{n-k-L} = e^{j2\pi\Delta FLT_s} \sum_{k=0}^{L-1} |r_{n-k}|^2 \qquad \text{Eq. IV.13}$$

Where (*) denotes the conjugate of the signal. The frequency offset could be estimated as:

$$\Delta\hat{F} = \frac{1}{2\pi LT_s} \tan^{-1}\left[e^{j2\pi\Delta FLT_s} \sum_{k=0}^{L-1} |r_{n-k}|^2 \right] \qquad \text{Eq. IV.14}$$

To minimise the effect of noise on the estimated frequency offset, the cross-correlation values were accumulated over the entire SYNC sequences. Figure IV-15 shows the schematic of the implemented carrier recovery. The cross-correlation was implemented with delays and complex multiplication. The accumulator is enabled only during the SYNC sequences and reset when the estimation for the current sequences is completed. The arctangent function performed with the arctangent IP-core provided by the Xilinx system generator. To compensate for the carrier frequency offset (CFO) a numerically controlled oscillator (NCO) synthesises a sinusoidal signal which is multiplied by the received signal in order to cancel the CFO.

With the phase width set to 32 bits, and amplitude resolution of 16 bits, the NCO will have a frequency resolution of 0.1 Hz and spurious-free dynamic range (SFDR) equals to 90 dB.

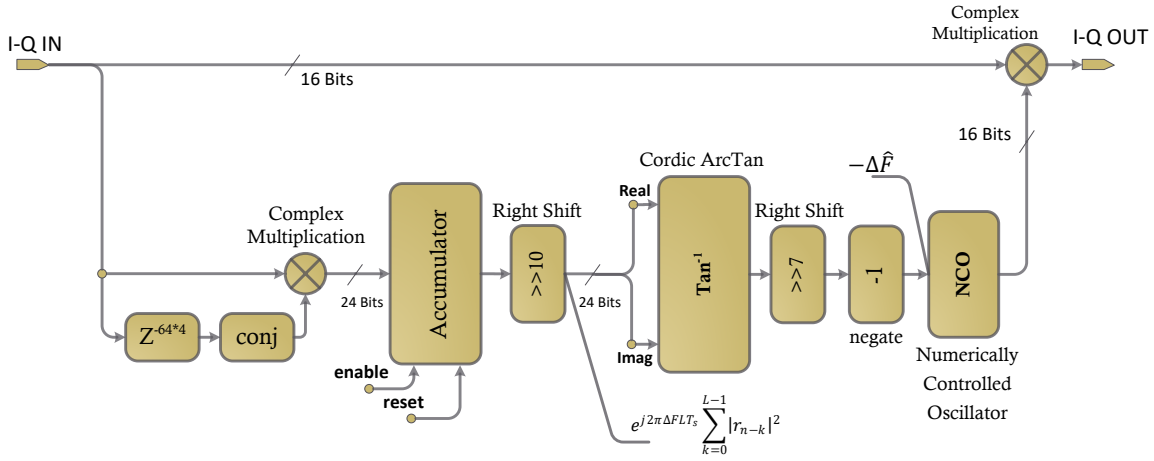


Figure IV-15 Schematic of the Carrier Recovery Module

IV.2.7 Root Raised Cosine Filters

Root raised cosine filter (RRC) is one of the most common shaping filters in radio design. The RRC is used to shape and limit the spectrum of the signal to cancel inter-symbol interference, where the received signal will have zero-crossing for each symbol's impulse response placed in such a way that at each sampling instant, the RRC provides an output signal that is due to only a single symbol. At the transmitter interpolation (up-sampling) is performed prior to filtering, a similar RRC filter is used in the receiver to keep only the band of interest to reduce noise and remove frequency images generated by the over-sampling at the ADC converter. The up-sampling is fixed to four times the original sample rate. Generally, digital RRCs are implemented as finite impulse response (FIR) rather than infinite impulse response (IIR) filters for reasons of stability. The degree to which the filter response matches the ideal one is dependent on two parameters: the up-sampling factor M and number of taps N (filter order). Generally, N is chosen to be an integer multiple of M, N=D×M, where D is an integer value[40]. Figure IV-16 plots the frequency and impulse responses of the implemented RRC filter, the up-sampling factor M equals to 4 and number of taps employed is 44 taps. The normalized bandwidth and roll-off factor equal to 0.35 and 0.1 respectively. Figure IV-17 shows the measured spectrum of the SC-FDE and OFDM transmitted signals when employing this RRC filter.

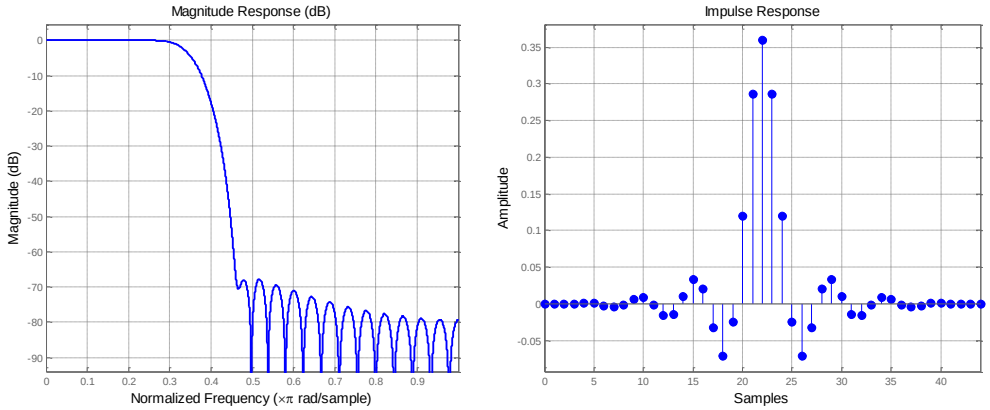


Figure IV-16 Frequency and Impulse Response of the Implemented RRCs

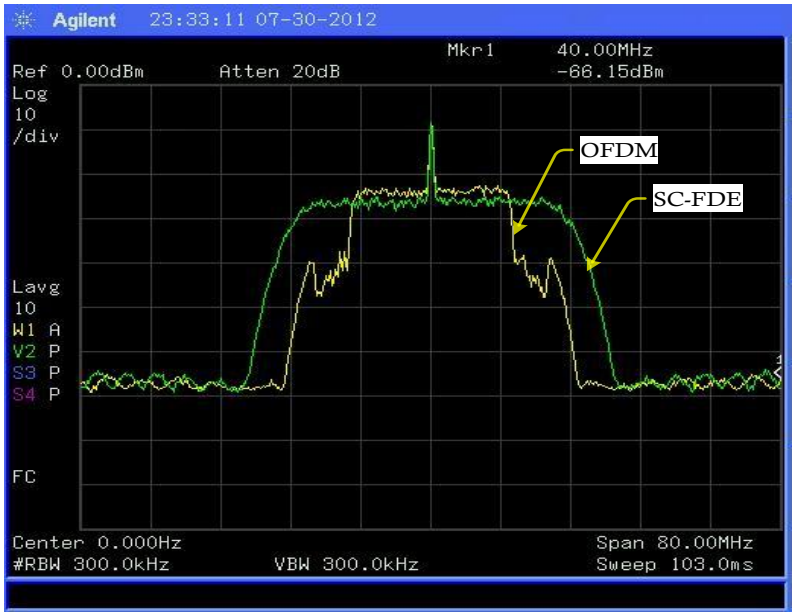
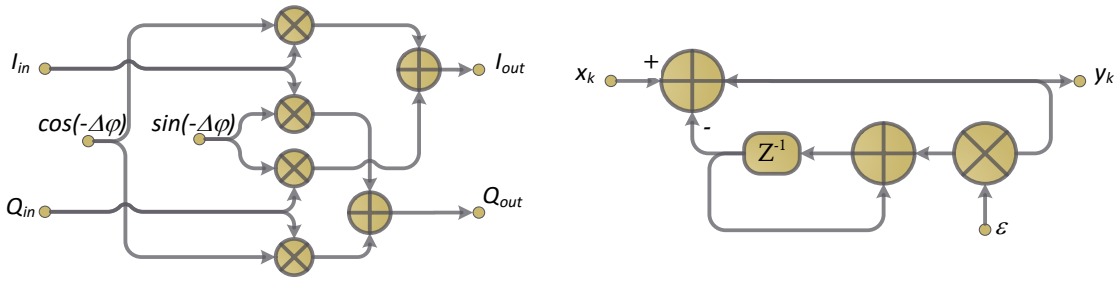


Figure IV-17 Measured Signal Spectrum of SC-FDE and OFDM

IV.2.8 DC Offset Cancelation and IQ Imbalance Compensation

Using quadrature mixers introduces further RF impairments such as IQ Phase/Gain imbalances and DC offset component. The phase and gain imbalances are attributed respectively to the phase and gain mismatch between the in-phase (I) and quadrature (Q) components. The dc offset could be originated from different analogue devices including amplifiers, RF mixers, and the analogue components of the ADC converters [20].

Because the gain imbalance is negligible, only phase imbalance is considered in this design, a digital pre-distortion applies an exact inverse of the imbalance distortion of the modulator before the analogue to digital conversion. Figure IV-18.a shows the pre-distortion schematic where the negated phase imbalance -Δφ is applied at the receiver. The dc offset can be removed at the receiver side before the ADCs using the DC-Blocker capacitors. The drawback of this method is that the lower frequencies of the baseband signal are attenuated which leads to a distortion of signal. An easy FPGA implementable digital method to eliminate the DC component is the DC-Canceller shown in Figure IV-18.b. The transfer function of this high-pass filter is $H_{(z)} = \frac{z-1}{z-(1-\epsilon)}$. Assigning a very small value to ε makes the cut-off frequency of this filter very close to zero to remove the DC component [58].



(a) (b)

Figure IV-18 Phase Imbalance Pre -Distortion (a) and Simple DC-Canceller (b)

IV.2.9 16-QAM Mapping/De-Mapping

Each four bits generated by the pseudo random generator are mapped using the 16-QAM constellation. The "In-phase" and "Quadrature" signals are generated from the first and the last two bits respectively according to Table IV.1. The four coding values (-3, -1, +1 and +3) are stored in a read only memory (ROM). The resolution employed to generate the IQ components is 16 bits, the block diagram of 16-QAM mapping is shown in Figure IV-19 [59].

Table IV.1 The 16-QAM Mapping Table

B_0B_1	In Phase (I)	B_2B_3	Quadrature (Q)
00	-3	00	-3
01	-1	01	-1
10	1	10	1
11	3	11	3

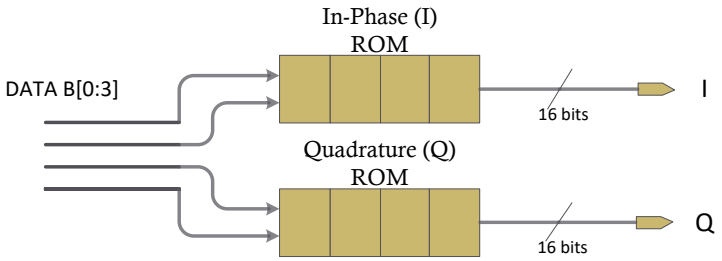
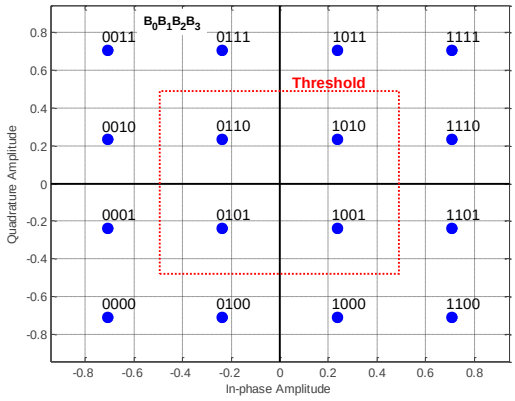


Figure IV-19 ROM Based 16-QAM Mapping

At the receiver, and to perform the 16-QAM de-mapping of the received IQ baseband signal a Matlab code is implemented. The received IQ signals are assigned to the nearest point in the IQ constellation; therefore, I and Q signals are compared to a predefined threshold which is set at the mid-way between two neighbouring points. Figure IV-20 illustrates this principle. The implementation of the De-Mapping code is based on the Xilinx "M-Code" block that contains MATLAB code to be executed within Simulink to calculate the block outputs during simulation. The same code is translated into equivalent behavioural HDL code when hardware is generated [59].




```
function [B3,B2,B1,B0,dv] = sdr_qam16_dem(I, Q, En, THR);
if (En)
  if (I > 0)
    if (I > THR)
      B2 = xfix({xlUnsigned, 1, 0}, 0);
      B3 = xfix({xlUnsigned, 1, 0}, 1);
    else
      B2 = xfix({xlUnsigned, 1, 0}, 1);
      B3 = xfix({xlUnsigned, 1, 0}, 1);
    end
  else
    if (I > -THR)
      B2 = xfix({xlUnsigned, 1, 0}, 1);
      B3 = xfix({xlUnsigned, 1, 0}, 0);
    else
      B2 = xfix({xlUnsigned, 1, 0}, 0);
      B3 = xfix({xlUnsigned, 1, 0}, 0);
    end
  end
  if (Q > 0)
    if (Q > THR)
      B0 = xfix({xlUnsigned, 1, 0}, 0);
      B1 = xfix({xlUnsigned, 1, 0}, 0);
    else
      B0 = xfix({xlUnsigned, 1, 0}, 1);
      B1 = xfix({xlUnsigned, 1, 0}, 0);
    end
  else
    if (Q > -THR)
      B0 = xfix({xlUnsigned, 1, 0}, 1);
      B1 = xfix({xlUnsigned, 1, 0}, 1);
    else
      B0 = xfix({xlUnsigned, 1, 0}, 0);
      B1 = xfix({xlUnsigned, 1, 0}, 1);
    end
  end
  dv = xfix({xlBoolean}, 1);
else
  B0 = xfix({xlUnsigned, 1, 0}, 0);
  B1 = xfix({xlUnsigned, 1, 0}, 0);
  B2 = xfix({xlUnsigned, 1, 0}, 0);
  B3 = xfix({xlUnsigned, 1, 0}, 0);
  dv = xfix({xlBoolean}, 0);
end
end
```

Figure IV-20 16-QAM De-Mapping Decision Scheme, and its Matlab Code Implementation

IV.2.10 Forward Error Control (FEC)

As specified in the IEEE 802.15.3c standard, in the SC-FDE communication scheme reed Solomon (RS) is adopted, with code rates equals to 1/2, 3/4 and 7/8 with the respective code sizes: RS(200,100), RS(200,150), and RS(200,170).

The FEC has been enhanced by employing random byte-interleaving mechanism, where data bytes are re-arranged using random permutation, at the receiver a same permutation is employed to arrange the data to the original order.

Matlab Simulink communication toolbox is employed to provide both RS coding blocks, and byte interleaving. Hence, the coding at the transmitter and decoding at the receiver run on the personal computer (PC).

IV.2.11 SC-FDE/OFDM Design Considerations

As shown in Figure IV-1, the only difference between SC-FDE and OFDM is the placement of the IFFT, which in OFDM systems used at the transmitter to generate modulated subcarriers. However, and in order to reduce out-of-band emission, and thus relaxes the frontend filters requirements, the subcarriers near the edge, known as guard subcarriers, are made null, in addition, some of subcarriers around DC frequency are made null as well to cancel the DC offset and unwanted low-frequency components originated from RF frontend [60].

As shown in Figure IV-21.a, 100 out of 128 subcarriers are employed to carry data, the index zero subcarrier (dc subcarrier) and the remaining subcarriers are fixed to zero value, the output signal spectrum, shown in Figure IV-21.b, contains subcarriers' images that could be easily removed through a root raised cosine filter.

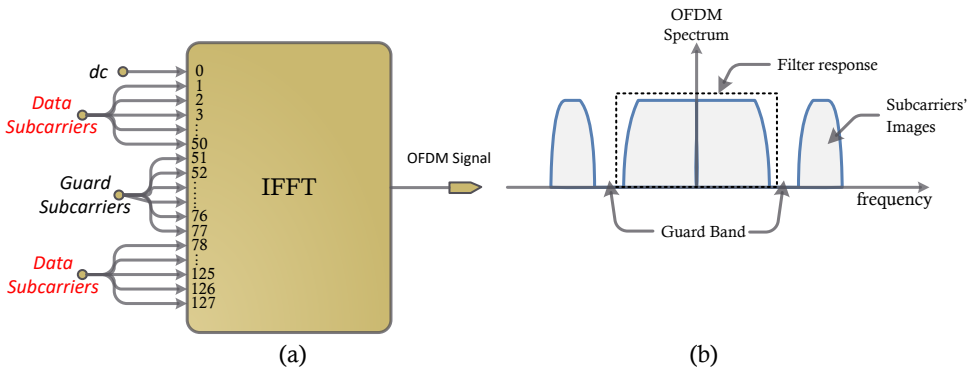


Figure IV-21 OFDM Subcarriers Mapping (a), and the Resulting Spectrum (b)

In SC-FDE, no IFFT is involved in the transmitter; zero-padding (ZP) is applied where the guard interval (GI) and 28 out of 128 data samples are filled with zeros as shown in Figure IV-22. Guard interval and zero padding intervals serve to separate two successive data sub-blocks to avoid inter-blocks interference (IBI), and helps suppressing adjacent channel interference [61].

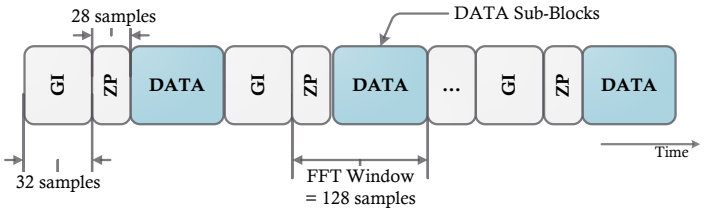


Figure IV-22 SC-FDE with Zero-Padding (ZP)

To summarize, the specifications of the implemented SC-FDE/OFDM transceiver are shown in Table IV.2. Due to the overlapped subcarriers, the OFDM signal has narrower bandwidth than the single carrier signal in SC-FDE mode. Employing the 16-QAM modulation scheme, the same maximum data rate of 100 Mb/s is achieved in both SC-FDE and OFDM communication schemes, with a spectrum efficiency of 2.8 and 5 bit/s/Hz in SC-FDE and OFDM respectively.

Table IV.2 SC-FDE and OFDM System Parameters

Parameters	Specification	
	SC-FDE	OFDM
Signal Bandwidth	35 MHz	20 MHz
Spectrum Efficiency	2.8 bit/s/Hz	5 bit/s/Hz
FFT Size (N)	128	
Guard Interval (GI) Length	32	
Channel Impulse Response Length	128	
CES Repetition (M)	4	
Modulation	16-QAM	
Maximum Bit-rate	100 Mb/s	

IV.3 Hybrid FPGA/GPP Platform for SC-FDE/OFDM Implementation

The baseband signal processing functions of the millimetre-wave radio transceiver developed and employed in the experiments reported in this thesis is based on software-defined radio (SDR) approach (i.e., signal processing tasks run in a programmable digital signal processing engine).

For this purpose, the 'XtremeDSP' Development Kit-IV from Nallatech is used as development platform that employs the Xilinx Virtex-IV FPGA technology. The

development Kit uses dual channel, high performance ADCs and DACs, as well as a user programmable Virtex-IV device [62].

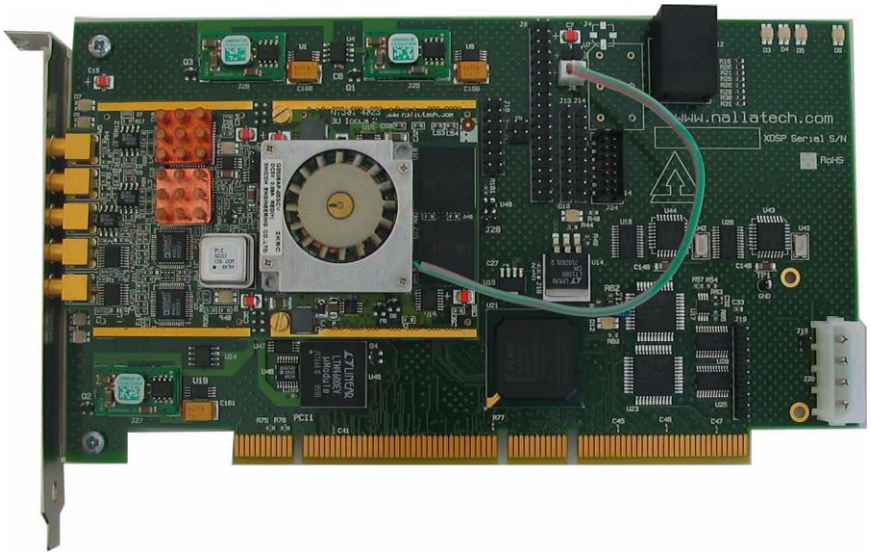


Figure IV-23 XtremeDSP Development Kit-IV [62]

Shown in Figure IV-23, the 'XtremeDSP' development board consists of a motherboard populated with a module (daughter card). The motherboard is referred to as the "BenONE-Kit Motherboard" and the module is referred to as the "BenADDA DIME-II module". The key Hardware features of the Kit include:

- Xilinx Virtex-IV User FPGA: XC4VSX35-10FF668,
- 2 independent ADC channels, AD6645 ADC (14-bits up to 105 MSPS),
- 2 independent DAC channels, AD9772 DAC (14-bits up to 160 MSPS),
- Support for external clock, on board oscillator, and programmable clocks,
- Host interfacing via 3.3V/5V PCI 32-bit/33-MHz interface,
- Spartan-II FPGA for 3.3V/5V PCI Interface.

Exploiting the PCI Bus, which allows data exchange between the development board and the host PC, a hybrid platform built with on board FPGAs and general purpose processor (GPP) is adopted. Figure IV-24 shows the software-radio hybrid platform employed to implement the proposed SC-FDE/OFDM baseband transceiver.

This hybrid platform employs FPGAs for baseband signal processing to perform filtering, equalization, and correlation functions with high throughput and optimal performance, and a GPP processor to run the forward error control (FEC), this

includes reed Solomon (RS) coding and interleaving tasks which require complex decoding algorithms. These algorithms deal with frames of integers and logic operations; hence, performance is not a key factor.

The 2-channels analogue to digital converter (ADC) and digital to analogue converter (DAC), clocked at 100 Ms/s by the Virtex-II FPGA, are utilized to interface the digital signal processing modules with the analogue IQ baseband signals. The digital baseband transmit/receive signals are synthesized/processed by the Virtex-IV FPGA by digital signal processing functions that run in fully pipelined fashion at 100 MHz

An auxiliary Spartan-II FPGA connects the main Virtex-IV FPGA with the host PC through the PCI Bus. The host PC has a dual-core GPP processor and runs at 1.2 GHz. The Host PC is employed to implement the FEC algorithms, generates random data for test purposes, and loads reconfiguration files into the FPGA.

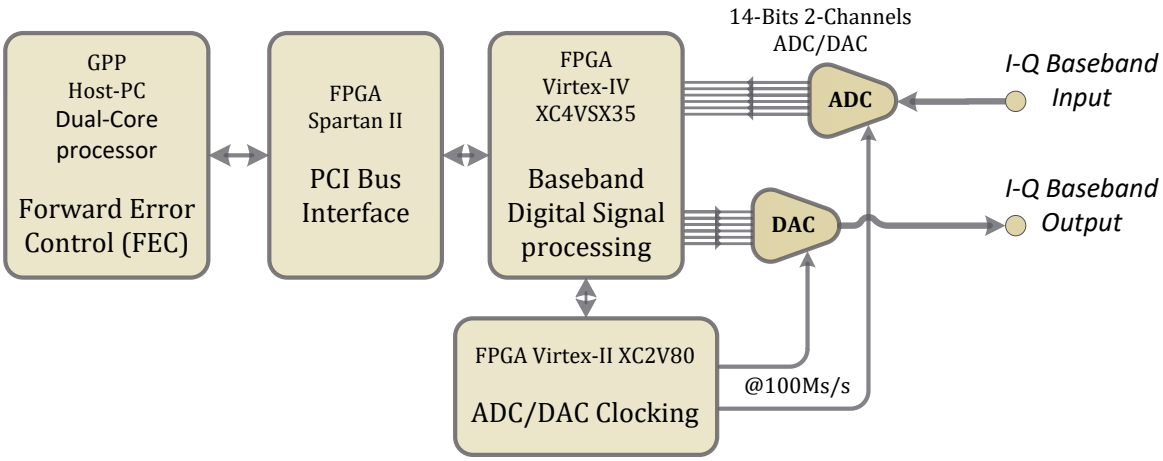


Figure IV-24 Block Diagram of the Software-Defined Radio Platform

IV.4 FPGA Implementation

Once the full baseband transceiver design completed, the system generator automatically translates the design into VHDL code, then synthesises, places, and routes the VHDL code to generate FPGA bitstream along with a Simulink library that stores the hardware co-simulation block. Figure IV-25 shows the dialog box when synthesising a hardware co-simulation block.

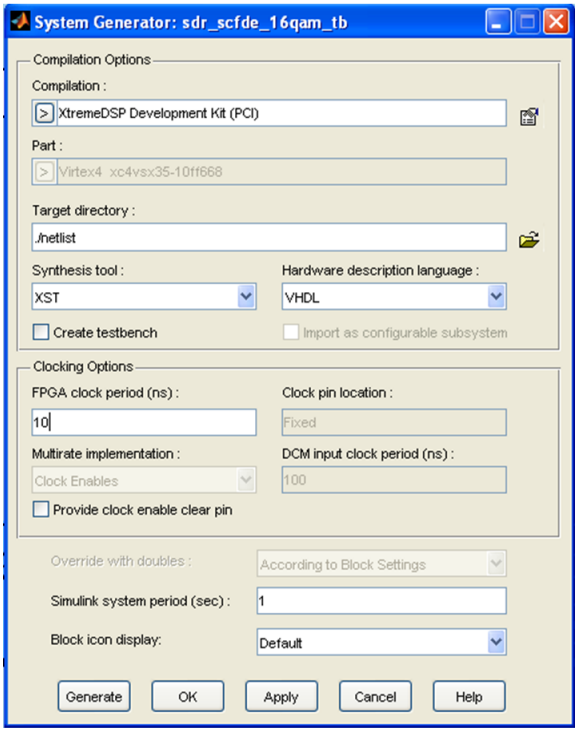


Figure IV-25 System Generator Tool to Synthesis a Hardware Co-Simulation Library

The hardware co-simulation block is then used in Simulink design like any other block is used. During simulation, the hardware co-simulation block interacts with the FPGA board, automating tasks such as FPGA configuration, data transfers, and clocking. The hardware co-simulation block has inputs and outputs, so when a value is written to one of the block's input ports, the block sends the inputted data to the appropriate location in the hardware. Similarly, the block retrieves data from the hardware when there is an event on an output port [45].

Another efficient way to exchange data between host PC and FPGA board is the shared memories, where in this case hardware co-simulation interface allows shared memory block and its derivatives (e.g., shared FIFO and shared Registers) to be integrated in the FPGA and mapped transparently to common address spaces on the host PC. Hence, shared memories can help facilitate high-speed data transfers between the host PC and FPGA, and provide a tool for real-time hardware co-simulation [45]. Figure IV-26 shows an example of hardware co-simulation design, FIFOs memories are employed to exchange data between the host PC and FPGA device or exchange a single value with shared registers.

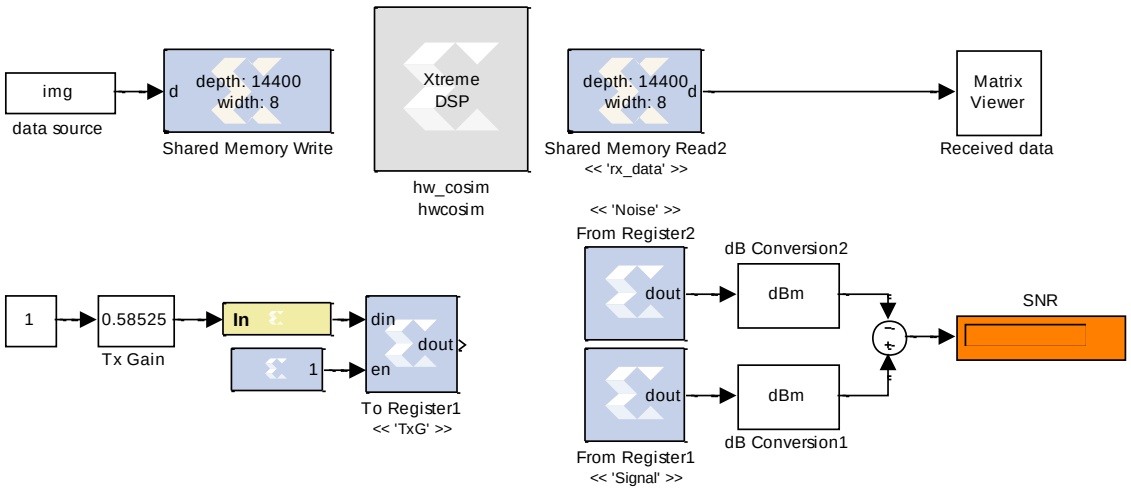


Figure IV-26 System Generator Hardware Co-Simulation with Shared Memory

Table IV.3 gives the amount of FPGA resources consumed in each module and the full design. The first remark is that most of the consumed resources are used by the FDE equalizer, this due to divisions, several multiplications, and FFT/IFFT transforms, which are functions that need huge resources. The full design in either SC-FDE or OFDM mode, consumes around 80 % of the available FPGA resources, and a maximum frequency clock is 115 MHz with a dissipated power of 1.22 Watt.

Table IV.3 Resources Used in Different Modules and Full Design, Max Throughput and Dissipated Power on Virtex-IV FPGA

Resources	FDE Equalizer	Carrier Recovery	AGC	RRC Filters	SYNC and SFD Frames Detector	Used/Available (Full Design)	% Resources Used
Flip Flops (FFs)	17,406	537	1,022	416	524	**20,164** /30,720	65 %
Lookup Tables (LUTs)	19,329	1,306	1,360	314	546	**23,442** /30,720	76 %
Logic Slices	11,440	852	881	338	354	**13,659** /15,360	88 %
DSP48s/Embedded multipliers	44	8	5	24	2	**181** /192	94 %
Embedded RAMs	8	2	-	-	-	**16** /192	8 %
						Max Throughput (MHz)	115 MHz
						Dissipated Power (W)	1.22 W

IV.5 Conclusion

So far, the two communication schemes SC-FDE and OFDM have been designed and implemented on the XtremeDSP Development Kit-IV with Virtex-IV FPGA. In order to achieve the highest data rate of 100 Mb/s and operate within an acceptable performance, the 16-QAM modulation scheme was adopted. The modular structure of the proposed transceiver has been described in details module by module, and a functional analysis of each module with their respective FPGA implementation, the resources utilization of the full design has shown about 80% of the available FPGA resources. The system generator implementation of those modules is included in Appendix A.

Furthermore, the FPGA design has been extended to include the forward error control (FEC), where it has been proposed to be implemented on the host PC using Matlab Simulink library.

CHAPTER V
Hardware and Experimental Setups

V.1 Introduction

In this chapter, the 64.8 GHz millimetre-wave wireless link is presented. The millimetre-wave transceiver interfaced with the implemented 16-QAM SC-FDE/OFDM baseband module, described in CHAPTER IV, is then discussed.

The completed 64.8 GHz wireless system is used to perform experiments in a number of indoor channels in order to characterize the bit-error rate (BER) performance against signal-to-noise ratio (SNR) in line-of-sight (LOS) and non-line-line-sight (NLOS) condition. Measurements were conducted in typical furnished office/desktop and long narrow corridor using a combination of omnidirectional and directional antennas.

The proposed radio channels employed in the measurements, closely replicate the transmission conditions encountered in a number of potential applications (e.g., uncompressed video streaming, backhaul, ad-hoc etc). Those applications are defined as "use cases" in the IEEE 802.15.3c standard [53].

V.2 The 64.8 GHz Millimetre-Wave Radio System

The RF and the analogue frontend of the millimetre-wave transceiver are built with commercially available discrete components as shown in the block diagram of Figure V-1.

At the transmitter the in-phase (I) and the quadrature (Q) components of the baseband signal are modulated onto a 2.4 GHz intermediate frequency through a Quadrature Mixer (IQ Mixer), the intermediate carrier is obtained from a phase locked oscillator (PLO) which was synthesised from an external 10 MHz crystal.

The IQ mixer's output was passed through a bandpass filter and applied to a 64.8 GHz millimetre-wave up-converter. The up-converter employed a 62.4 GHz local oscillator signal which was generated from a 10.4 GHz PLO synthesised from an external 100 MHz crystal. The 10.4 GHz was doubled and then tripled to produce a 62.4 GHz local oscillator signal. The 10.4 GHz PLO signal was split and fed into the receiver. The lower sideband signal centred around 60 GHz, at the output of the up-

converter, was suppressed using a band-pass filter centred at 64.8 GHz. Prior to transmission the upper sideband, centred at 64.8 GHz, was amplified by a 23 dB power amplifier.

At the receiver, the inverse process was performed, where the received signal is amplified using a low noise amplifier followed by a down-converter which had the 62.4 GHz LO signal connected to it. The 62.4 GHz signal was generated in the same way as that at the transmitter from the 10.4 GHz PLO. The down-converted signal at 2.4 GHz was then amplified using a 25 dB power amplifier. The analogue baseband IQ components were then detected using IQ Mixer, and passed through low-pass filters to remove any out-of-band frequencies; the baseband components are then digitized and processed by the digital baseband modules.

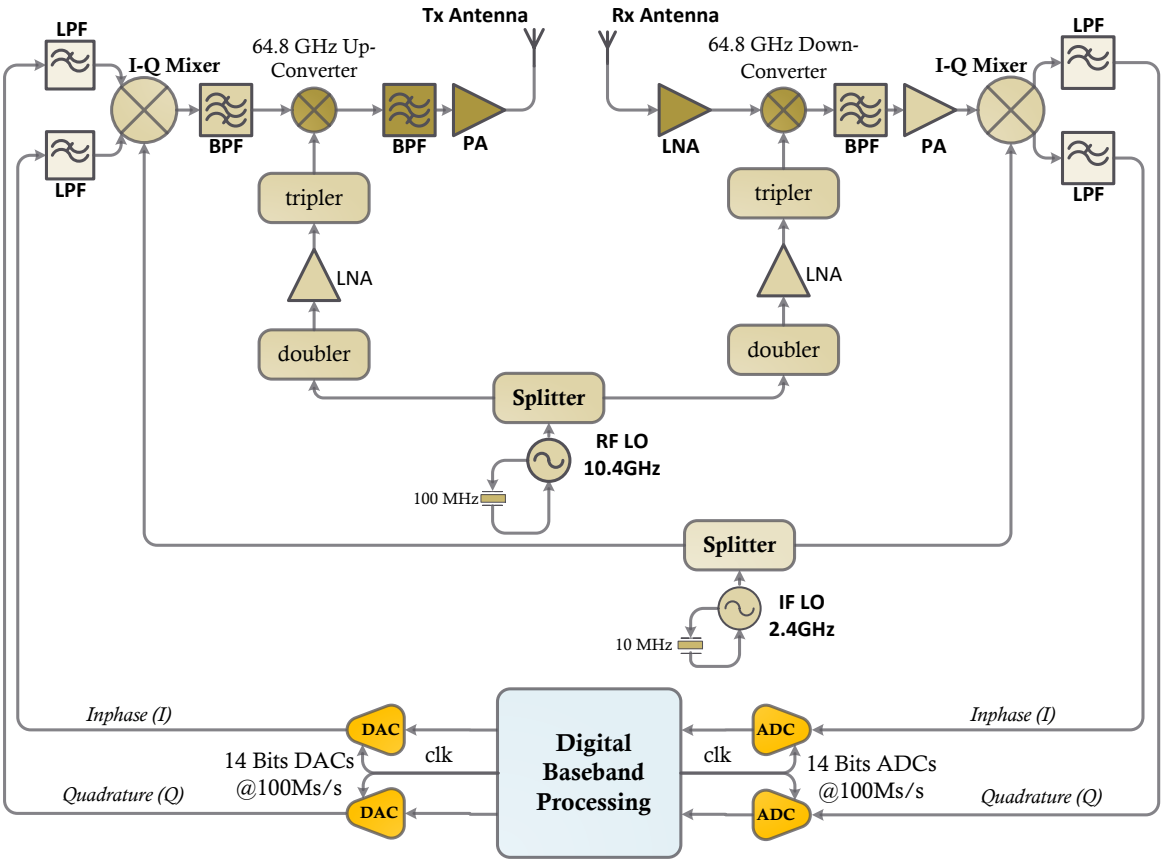
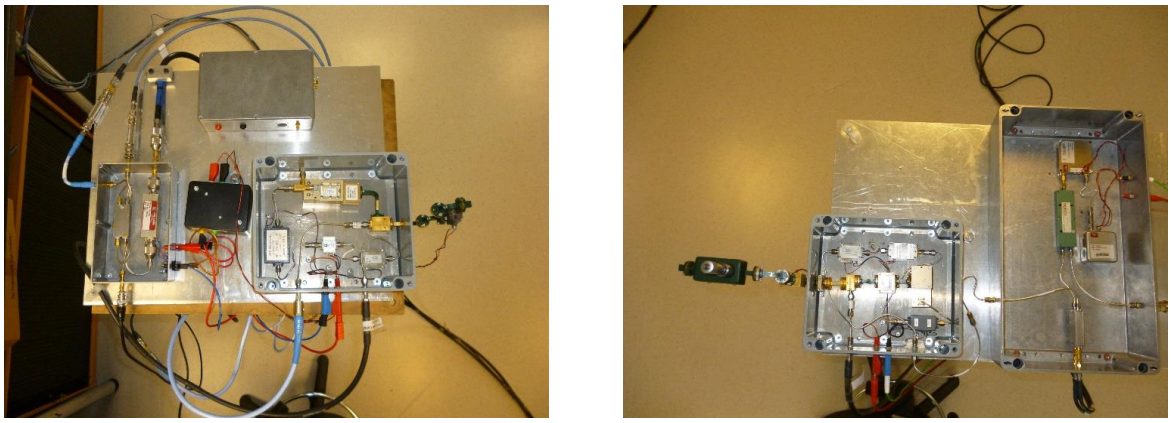


Figure V-1 The 64.8 GHz Millimetre-Wave Radio System Interfaced with the Baseband Module



Receiver Transmitter

Figure V-2 Hardware of the Millimetre-Wave 64.8 GHz Transceiver

V.3 BER Performance in Back-to-Back Configurations

Before evaluating the performance of the implemented millimetre-wave transceiver over real indoor channels, the digital baseband module that runs at 100 Mb/s has to be characterized in known conditions. Hence, the bit-error rate (BER) against estimated signal-to-noise ratio (SNR) has been evaluated over a number of back-to-back configurations shown in Figure V-3. Based on the Golay sequences, the estimation of the SNR along with the channel estimation have been performed at the receiver as explained in Section IV.2.3

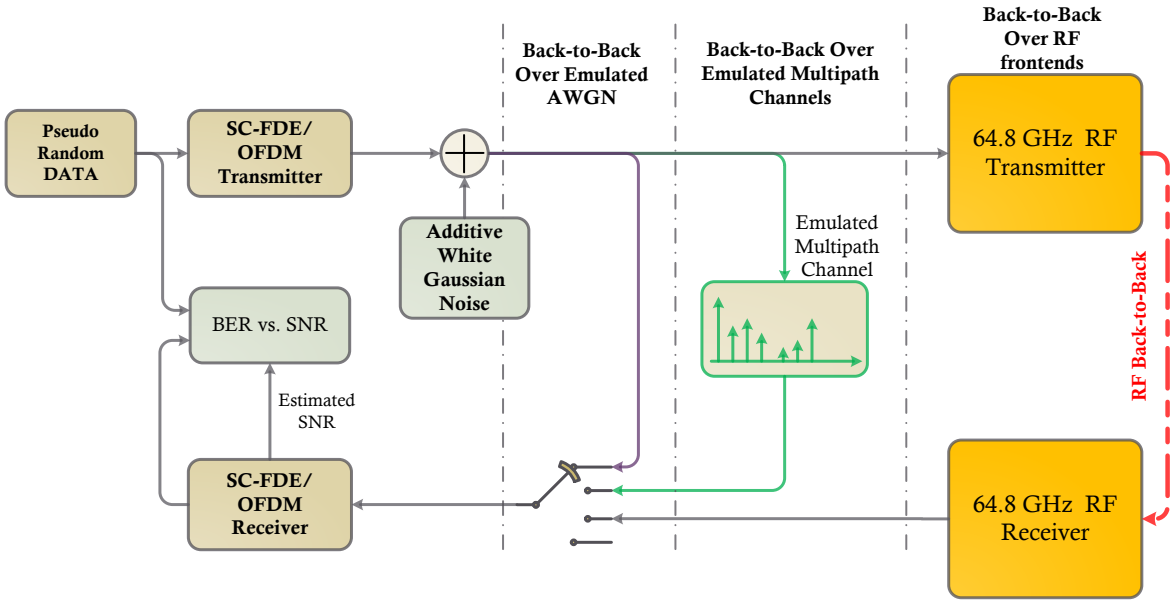


Figure V-3 Test-Bed for the 100 Mb/s Baseband with Different Back-to-Back Configurations

V.3.1 Characterization over Emulated AWGN/Multipath Channels

The first test is performed only on the baseband module, obtained by connecting the baseband IQ input/output signals in back-to-back loop. In both SC-FDE and OFDM communication schemes the baseband receiver employs similar frequency domain equalization.

An additive white Gaussian noise (AWGN) channel is realized by adding a power adjustable white Gaussian noise to the output IQ signals; this emulates the inherent thermal noise of any wireless system. Adjusting the noise level, an average of BER against the estimated SNR is then evaluated.

The AWGN channel is based on Xilinx white Gaussian noise generator (WGNG) IP-core, this generator generates white Gaussian noise using a combination of the Box-Muller algorithm and the central limit theorem [63].

Secondly, multipath propagations of millimetre-wave indoor channels was considered, the AWGN channel was cascaded with the emulation of a number of multipath channels, The emulated channels were implemented on the FPGA through a finite impulse response (FIR) filter and parameterized with the respective impulse response.

Based on the channel model adopted by the IEEE 802.15.3c standard, the emulated multipath channel reflects the multipath propagations within residential, desktop, and office with line-of-sight (LOS) and non-line-of-sight (NLOS) transmissions. Those are the typical residential CM1.1 LOS, residential CM2.1 NLOS, and desktop CM8.2 NLOS indoor channels with different multipath severity. Figure V-4 shows a snapshot of the impulse and frequency responses of the employed multipath channel models [9].

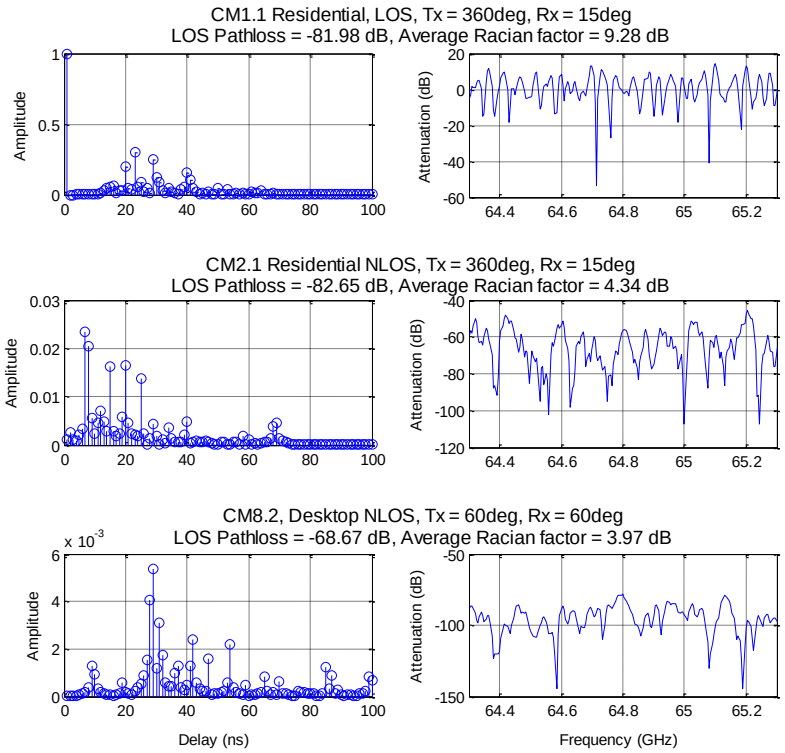


Figure V-4 Impulse and Frequency Response of the IEEE 802.15.3c Channel Models

Figure V-5 shows the BER vs. SNR over AWGN, and the emulated multipath channels CM1.1 LOS, CM2.1 NLOS, and CM8.2 NLOS, for both SC-FDE and OFDM. Over AWGN channel, the SNR required to achieve a BER probability of 10^{-6} in SC-FDE is around 24.6 dB, whereas, in OFDM the BER of 10^{-6} is achieved with a higher SNR that equals to 25.38 dB. This due to the fact that single-carrier has limited number of signal levels (i.e., four levels in 16-QAM). However, OFDM signal has quasi-infinite levels (continuous signal), thus, the OFDM signal experiences a higher distortion when converted to digital signal, due to limited number of bits in the ADC converter (14 bits).

Over multipath channels, the BER vs. SNR performance relative to that obtained in AWGN channel, demonstrate that the frequency domain equalization (FDE) technique employed in the receiver is effective in mitigating the effects of multipath propagation. In SC-FDE the FDE equalization totally cancels the multipath effect with only 0.4 dB is required above to that of AWGN channel to achieve 10^{-6}, over CM2.1 channel which has the highest LOS path loss of -82.65 dB.

In OFDM, the BER vs. SNR results show a degradation of the performance compared to that obtained for SC-FDE. For CM2.1 channel, a BER of 10^{-6} the SNR is 2 dB above that of an AWGN channel is required.

To summarize those results, Table V.1 shows the SNR penalties to achieve the maximum allowable BER of 10^{-6}, for different multipath channels in both SC-FDE and OFDM system. The discrepancy between SC-FDE and OFDM is primarily due to digital signal processing errors which arise in fixed point calculation.

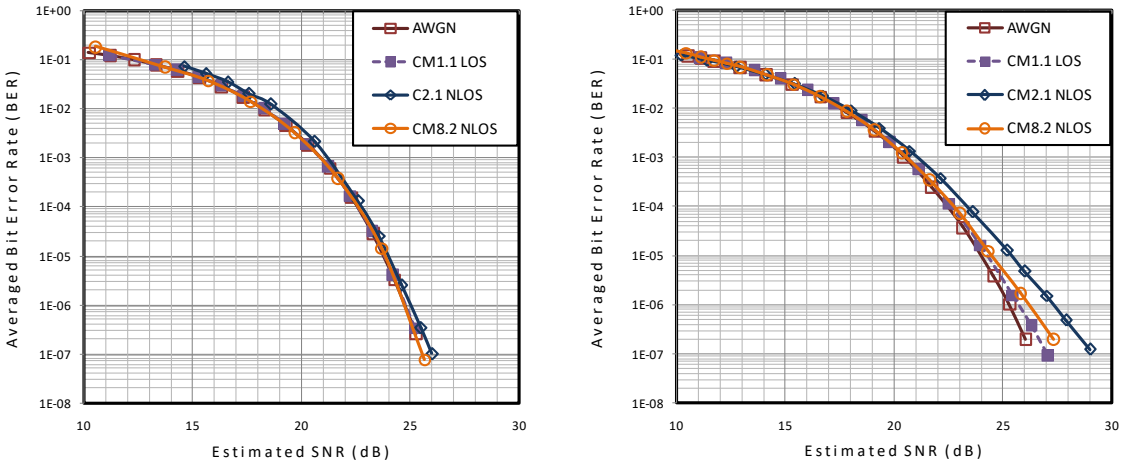


Figure V-5 BER vs. SNR over AWGN and Multipath Emulated Channels with SC-FDE and OFDM Communication Schemes

Table V.1 SNR Penalty Required to Achieve a BER of 10^{-6} over Multipath Channels

Channels	SNR Penalty to Keep BER = 10^{-6}	
	SC-FDE	OFDM
Residential line-of-sight (CM1.1)	0 dB	0.5 dB
Desktop non-line-of-sight (CM8.2)	0 dB	1 dB
Residential non-line-of-sight (CM2.1)	0.4 dB	2 dB

V.3.2 Characterization over the RF Frontend

In this case, the baseband module was connected with the 64.8 GHz millimetre-wave radio system as shown in Figure V-3. The effect of different imperfections (e.g., nonlinearity, phase noise, IQ imbalances, etc.) that characterize the RF frontend, are considered by a back-to-back loop of both transmit and receive antennas.

Figure V-6 shows the BER vs. SNR in both SC-FDE and OFDM, over AWGN (ideal RF frontend) and a transmission over the 64.8 GHz millimetre-wave frontend of Figure V-1. These results clearly show the robustness of the SC-FDE against the signal impairments caused by the RF frontend compared to the OFDM performance. Only 0.2 dB of extra SNR is required in SC-FDE to achieve 10^{-6} BER. While in OFDM system 2.6 dB of SNR is required above that of AWGN, this mainly due the high peak-to-average power ratio (PAPR) of the OFDM signal compared to single-carrier, which requires a larger power amplifier (PA) back-off.

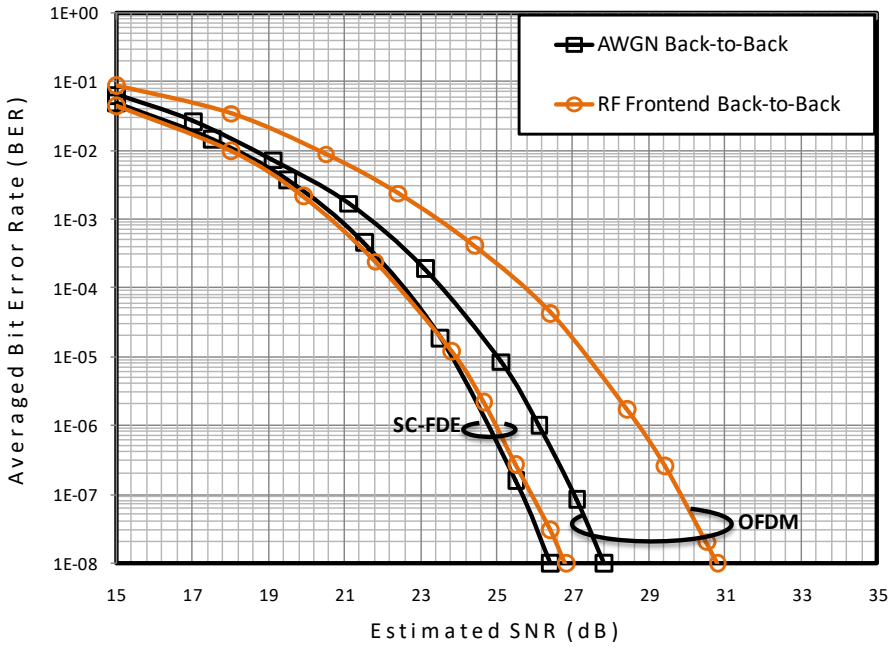


Figure V-6 BER vs. SNR over AWGN and RF Frontend Back-to-Back Loops

Another important parameter to characterise is the dynamic range of the implemented 64.8 GHz SC-FDE/OFDM receiver. The dynamic range of a receiver quantifies the maximum achievable distance while keeping constant performance.

The dynamic range has been characterized by connecting both terminals in back-to-back over RF frontend, and measuring the BER as a function of received signal power while maintaining a fixed SNR. Figure V-7 shows the dynamic range measured of both SC-FDE and OFDM with SNR of 18 dB and 20 dB respectively.

In SC-FDE the millimetre-wave receiver operates linearly over input signal powers in the range between -42 dBm and -58 dBm yielding a dynamic range of 16 dB. For received signal powers below -58 dBm the performance drops due to fact that the received signal power become comparable to the spurious components of the ADC

converter which leads to severe distortions. Those spurious signals are mainly due to the quantization noise and signal distortion, which are in their turn inversely proportional to the received signal power. However, powers larger than -42 dBm overdrive and saturate the LNA at the receiver frontend resulting in sharp degradation in BER performance.

In OFDM and due the high peak-to-average power ratio (PAPR) of an OFDM signal, high transmitted signal power is distorted, whereas in low signal power the ADC's spurious components highly distort the OFDM signal. Thus, only 6 dB of dynamic range is shown in OFDM, this poses huge obstacle to perform BER measurements in wide range of scenarios.

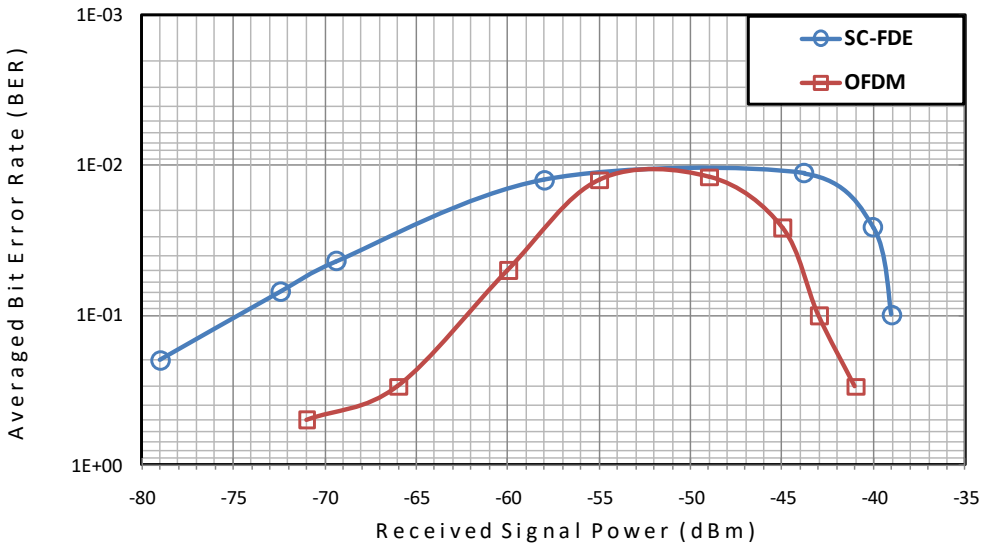


Figure V-7 Dynamic Range of the 64.8 GHz 16-QAM SC-FDE/OFDM Receivers

V.4 Conclusion

The implemented baseband transceiver with both SC-FDE and OFDM communication schemes has been tested against different distortions of the received signal. In the tests over emulated multipath channels with different multipath severities with LOS and NLOS conditions, the SC-FDE has shown a great robustness in mitigating multipath dispersion, with only 0.4 dB SNR penalty occurs in CM2.1 channel. This SNR penalty increases to 2 dB in OFDM system due to fixed point calculation errors that arise when processing a complex signal such as an OFDM signal.

The characterization of the dynamic range of both SC-FDE and OFDM has shown the capability to perform wide range of measurements in different scenarios. The SC-FDE

showed a dynamic range of 16 dB that is relatively larger dynamic range than OFDM with only 6 dB. This makes the OFDM unable to keep constant performance and cop against the fluctuations of the received signal power in different scenarios.

CHAPTER VI
BER Performance Characterization in Indoor Channels

VI.1 Introduction

To evaluate the robustness of the implemented SC-FDE/OFDM millimetre-wave communication system against both multipath channel dispersions, and imperfections of the RF frontend. Bit-error rate (BER) versus signal-to-noise ratio (SNR) performance has been characterized.

Experimental results of BER vs. SNR in LOS and NLOS conditions in a room and corridor are presented in this chapter and compared with those of AWGN channel in order to evaluate the effectiveness of SC-FDE and OFDM communication techniques to eliminate multipath propagation and cop with imperfections of the RF frontend.

VI.2 Indoor Environments Geometry

The performance of the implemented millimetre-wave transceiver system has been characterized by measuring BER vs. SNR in a rectangular room and a long narrow corridor for line-of-sight (LOS) and non-line-of-sight (NLOS) transmission scenarios.

The room was 6.9 metres long, 5.2 metres wide, and 2.61 metres high and it represents a typical furnished office/desktop. Two walls of the room had plasterboard surfaces, one was plasterboard with two 1.7 metres wide windows, and the fourth was plasterboard with a wooden door leading off to a narrow corridor. A bench, with a desktop located at one of its end, was mounted across one of the walls. The other walls had desktops, tables and cabinets alongside them as is shown in Figure VI-1. A photograph of the room is shown in Figure VI-2. The ceiling had fireboards suspended tiles with vinyl flooring.

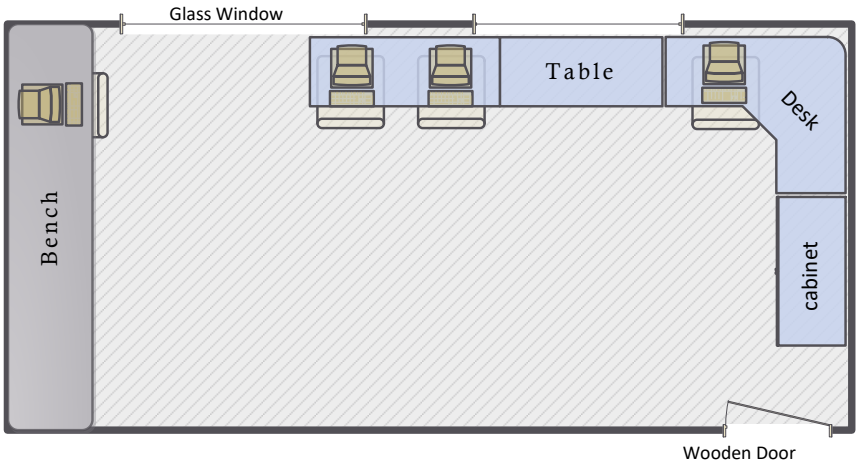


Figure VI-1 Geometry of the Rectangular Room (6.9×5.2×2.61 Metres)

Figure VI-2 Photograph of the Rectangular Room

The corridor's geometry is shown in Figure VI-3. The corridor (1.65 metres wide and 2.61 metres high) had 3 sections. Section A was 8.6 metres long, section B 6.8 metres long and section C 35 metres long. The corridor had plasterboard surfaces with a number of doorways leading off. However, one sidewall in section C was effectively glass. The ceiling had fibreboard suspended tiles and the floor was covered with a carpet as shown in Figure VI-4.

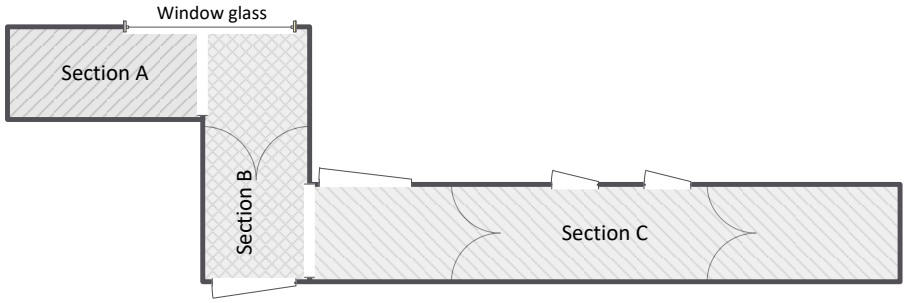


Figure VI-3 Geometry of the Narrow Corridor; Section A (8.6×1.65×2.61 metres), Section B (6.8×1.65×2.61 metres), and Section C (35×1.65×2.61 metres)

Section A Section B Section C

Figure VI-4 Photograph of Corridor's Sections

VI.3 Experimental Setups

A number of 64.8 GHz line-of-sight (LOS) and non-line-of-sight (NLOS) measurements with both SC-FDE and OFDM communication schemes were conducted at 100Mb/s. Measurements were done in room and corridor to characterise the BER performance of the millimetre-wave transceiver and its effectiveness in mitigating multipath propagation for different WPAN applications.

The considered transmission scenarios are defined relative to different use cases defined by the IEEE 802.15.3c [6].

VI.4 Antenna Configurations

The BER measurements with various antenna configurations were conducted to establish the effects of antenna directivity on the quality of 64.8 GHz wireless link. A combination of vertically polarized horn and omnidirectional transmit and receive antennas were employed.

The omnidirectional antenna, with 8 dBi of gain in the azimuth plane and an elevation beamwidth of 8°, consists of two plates supported by a plastic sheet around their circumference. The bottom plate, which is connected to a circular waveguide, has the shape of a cone, while the top one is a parabola. The horn antenna has a 10 dBi of gain with E and H elevation beamwidth of 55° and 69° respectively. Figure VI-5 shows photographs of the employed omnidirectional and horn antennas [64].

(a) (b)

Figure VI-5 The 8 dBi Omnidirectional (a) and 10 dBi Horn Antenna (b)

VI.5 BER Performance of the SC-FDE

Firstly, measurements in the room were made using 10 dBi horn antennas at both transmitter and receiver to closely represent the 802.15.3c U5 use case that describes office/desktop channels with fixed terminals, with LOS transmission and up to 5 metres apart, for file transfer and synch. The transmitter was located at one corner of the room with the receiver moved to 1, 2 and 4.5 metres away alongside the diagonal facing the transmitter. The measurement were repeated under identical conditions but with the transmitter located halfway across the room near to one wall with the receiver moved 1, 2 and 4.5 metres along a straight line facing the transmitter. These scenarios are referred to as U5-1m, U5-2m and U5-4.5m as depicted in Figure VI-6.

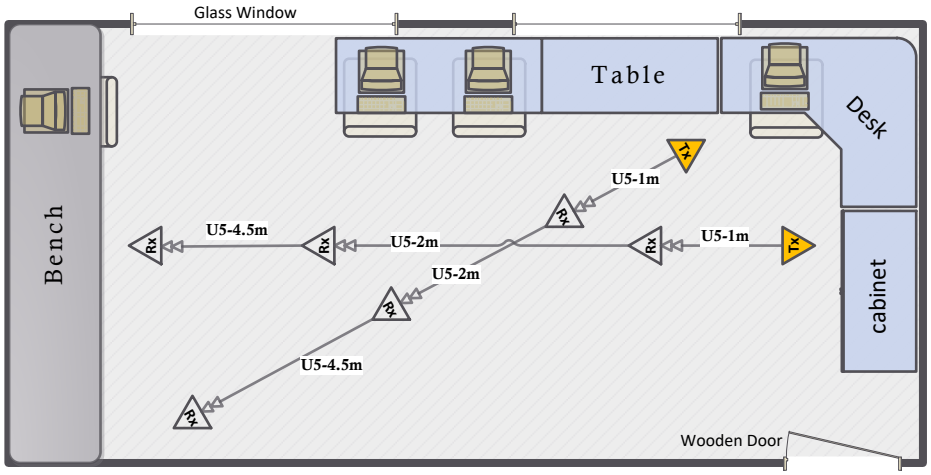


Figure VI-6 LOS Measurement Using Horn Antennas for Fixed Point-to-Point Applications (U5 Use Case)

The BER performance obtained at all separations, in the room, using transmit and receive horn antennas as illustrated in Figure VI-6 is shown in Figure VI-7. BER values measured along both routes with the terminals separated by the same distances are identical. Furthermore, the BER performance measured with the terminals 1, 2 and 4.5 metres apart are noticeably close to each other and closely represent BER values for AWGN channel. With the BER set at 10^{-6}, the required SNR is not more than 0.6 dB above that of the AWGN channel. This difference is primarily due to the processing error, as explained in CHAPTER V, as well as the nonlinearities of the RF components. In such U5 use case channels the FDE method is shown to be robust to eliminate multipath propagation in such environment.

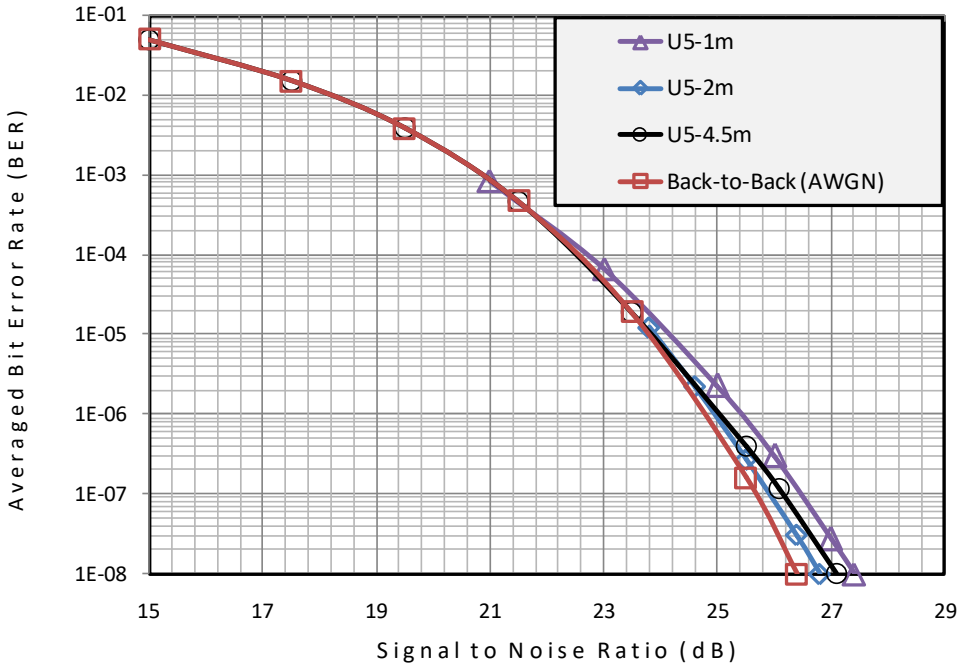


Figure VI-7 BER vs. SNR in SC-FDE for Line-of-Sight U5 Transmission with Horn Antennas

For ad-hoc applications in conference, office, and library experiments, where both terminals are portable as defined in the 802.15.3c U16 use case, measurements in the room were undertaken using omnidirectional antennas at both terminals. The transmitter and receiver were located at different locations in the room and at separations of 1, 2 and 4.5 metres. These scenarios are referred to as U16-1m, U16-2m and U16-4.5m as is depicted in Figure VI-8.

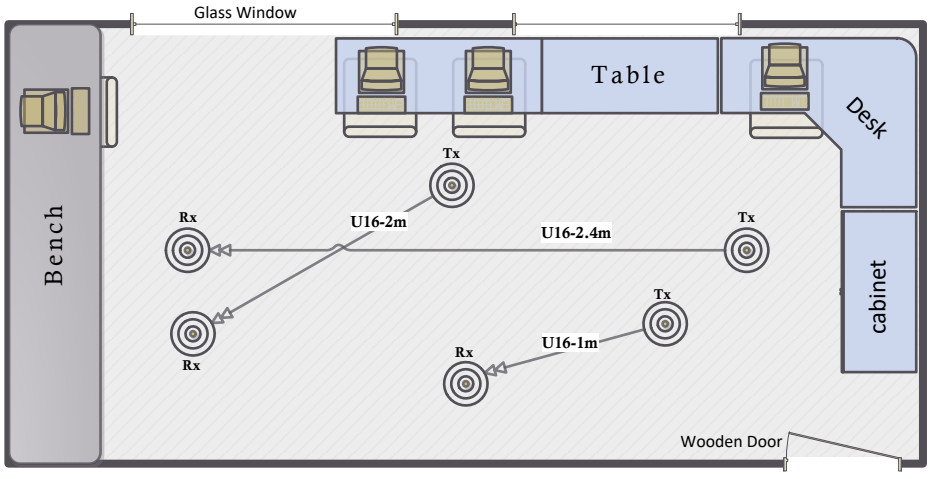


Figure VI-8 LOS Measurements Using Omnidirectional Antennas for ad-hoc (U16) Application

The third set of measurements in the room were made with the omnidirectional transmit antenna fixed in the middle of the room. The receiver, employing a 10 dBi

horn antenna, was moved to three different positions around the transmitter. This configuration reflects the U17 use case where the transmitter is an Ethernet or uncompressed video streaming access point located near the ceiling in an office, conference room or library, whereas the receiver is a portable device (e.g., laptop) with separations between 3 and 5 metres. These scenarios are referred to as U17-1m, U17-2m, and U17-3m as depicted in Figure VI-9.

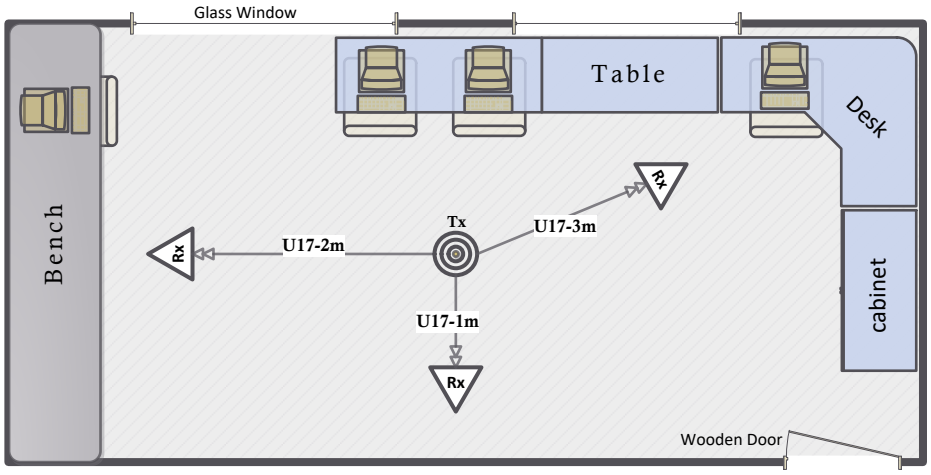


Figure VI-9 LOS Measurements for Fixed Omnidirectional Transmitter and Portable Directional Receiver

Results recorded in the room for use case U16 and U17, using omnidirectional transmit antenna as depicted in Figure VI-8 and Figure VI-9, show that the FDE equalization has also been successful in eliminating multipath fading where BER values close to those of AWGN are measured as is given in Figure VI-10 and Figure VI-11 respectively. With an omnidirectional receive antenna, the SNR penalty required to achieve a BER of 10^{-6} is not more than 1 dB greater than that needed in AWGN channel. Whereas, SNR penalty of 1.7 dB is measured when replacing the receive antenna with a horn.

The deviations from the AWGN values are because, with omnidirectional transmit antenna, the channel experiences more severe multipath propagation [65] which results in received signal power levels below the minimum required for the 64.8 GHz receiver to maintain a flat BER performance as characterized in Section V.3.2 and illustrated in Figure V-7.

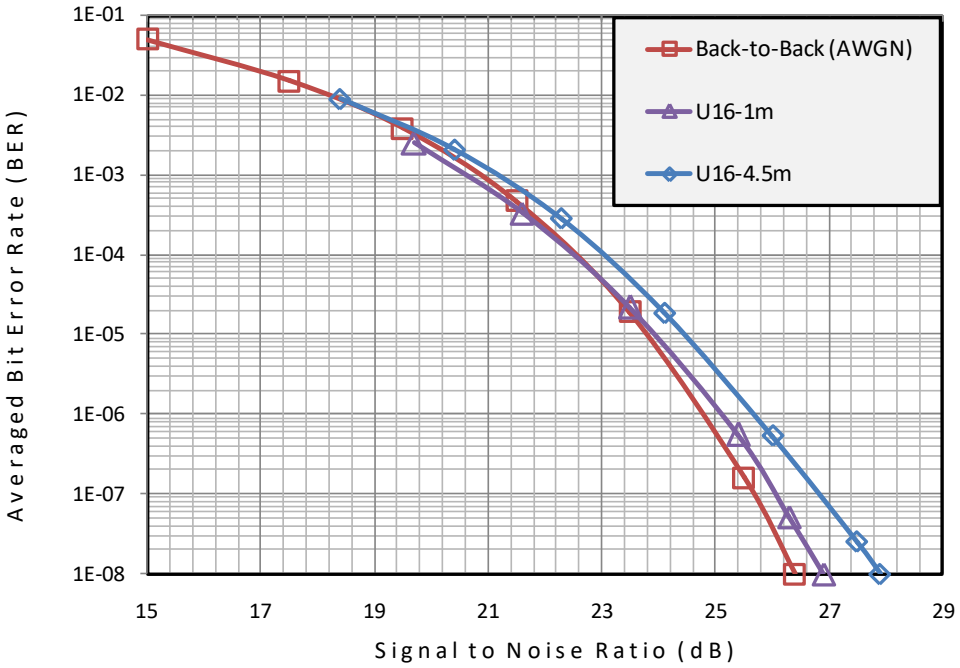


Figure VI-10 BER vs. SNR in SC-FDE for Line-of-Sight U16 Transmission with Omnidirectional Antennas

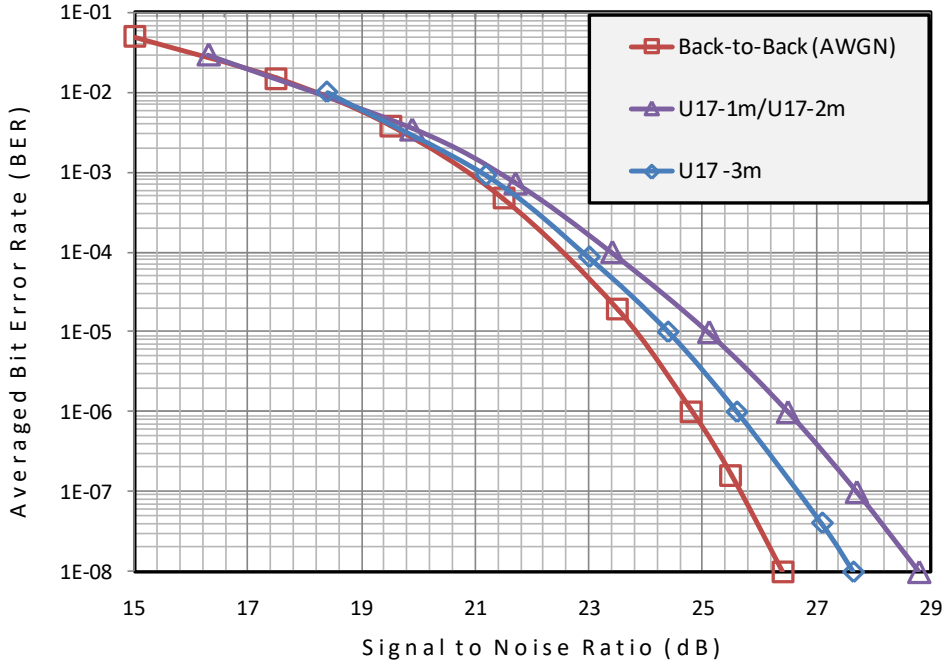


Figure VI-11 BER vs. SNR in SC-FDE for Line-of-Sight U17 Transmission with Omnidirectional Transmit and Horn Receive Antennas

A non-line-of-sight (NLOS) experiment with a scenario that closely represents the U8 use case, where the transmitter is a portable device and the receiver is a printer located somewhere in the room with NLOS condition was performed. The transmitter was positioned at two different locations with its horn antenna pointing at a wall or a corner of the room. The horn antenna at the receiver was pointed at the illuminated surface in such a way to measure reflections off the signal as is shown in Figure VI-12, these scenarios are referred to as U8-HH-1, U8-HH-2.

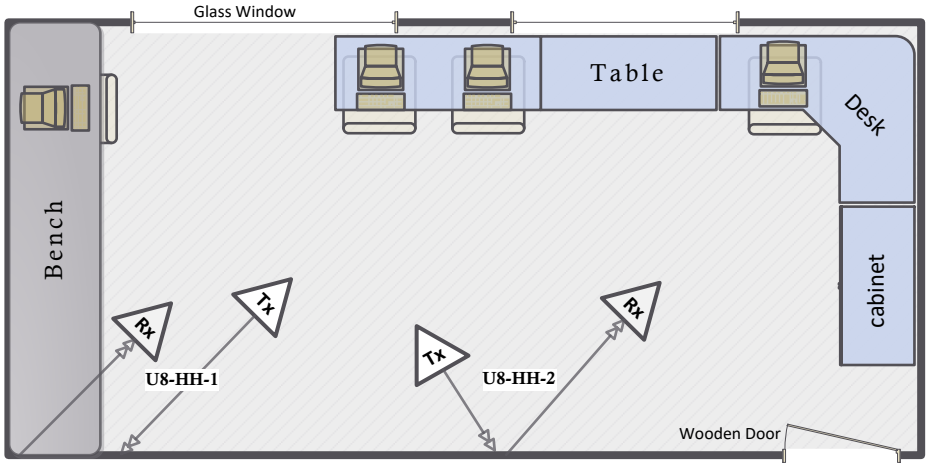


Figure VI-12 Obstructed LOS Scenario (U8) Using Horn-Horn Antennas

Furthermore, another NLOS measurement to represent the U1 use case, where transmit and receive antennas are omnidirectional but an obstacle such as wall or human body is temporally or permanently obstructs the LOS ray was performed. This was done by keeping the receiver inside the room, while taking the transmitter outside the room as is depicted in Figure VI-13. Measurements were repeated under identical conditions but at different receiver location alongside the wall.

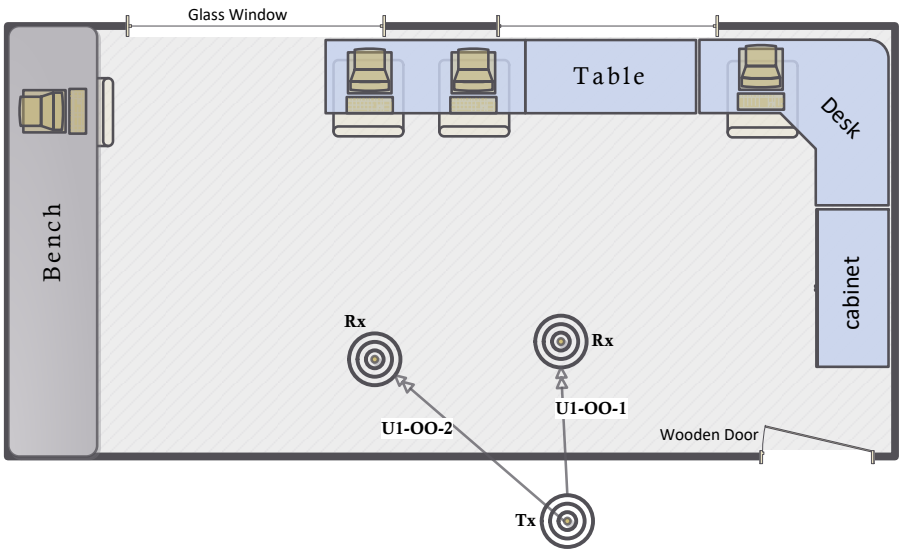


Figure VI-13 Obstructed LOS Measurements (U1) Using Omnidirectional Antennas

For NLOS transmission, BER results measured for use case U8 and U1 are illustrated in Figure VI-14 and Figure VI-15 respectively. Both cases show comparable results, with minimum and maximum SNR penalties relative to the AWGN channel are 0.8 dB and 3 dB respectively. This deviation from the AWGN channel performance is because the received signal power undergoes an important multipath fading propagation along with a strong attenuation in the absence of the LOS component. Thus, make the receiver operating outside the flat region of its dynamic range performance, resulting in the BER degradation.

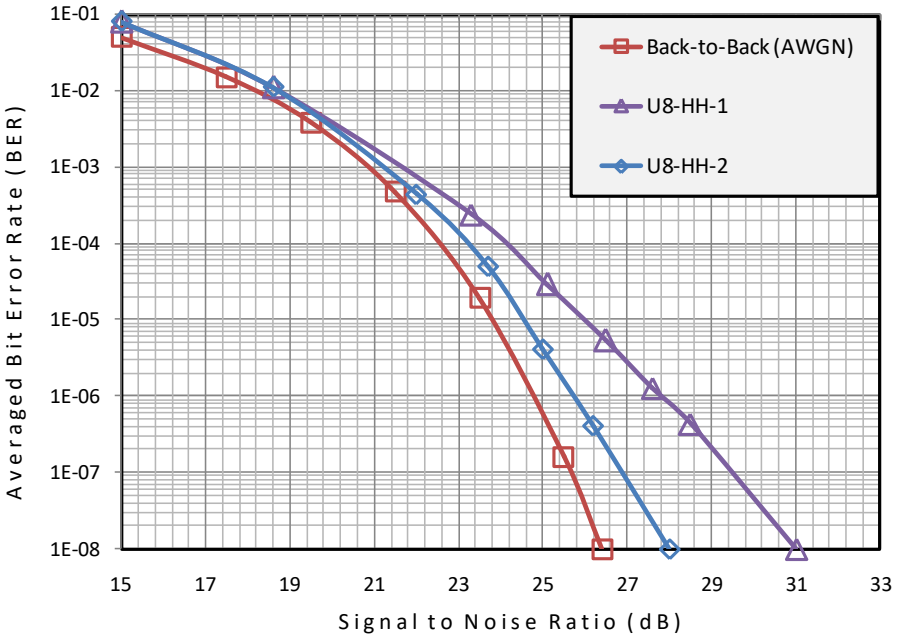


Figure VI-14 BER vs. SNR in SC-FDE for Reflexion Off the walls with Horn-Horn Antennas for Use Case U8

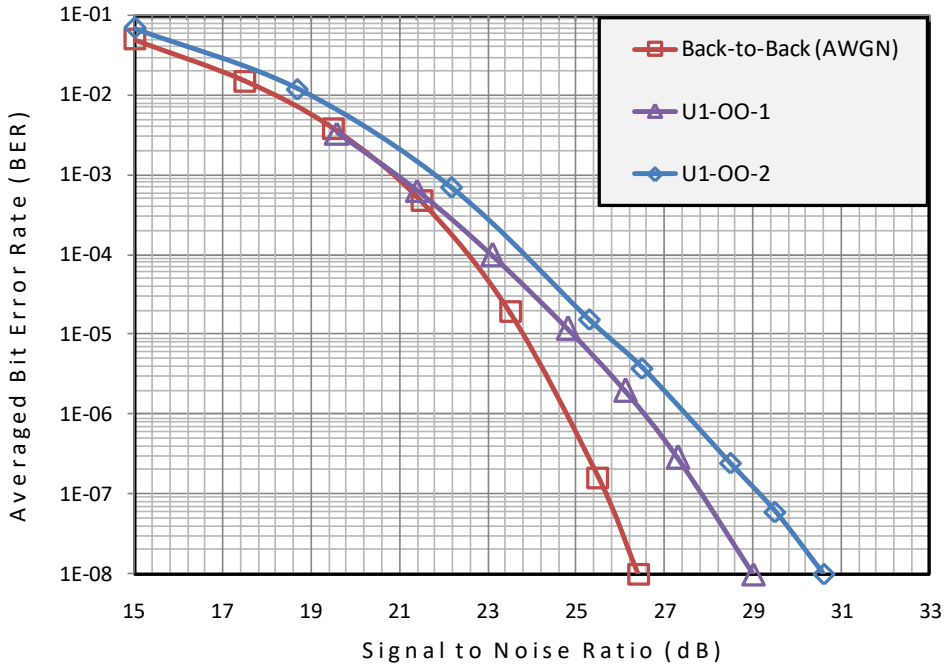


Figure VI-15 BER vs. SNR in SC-FDE for Obstructed LOS with Omni-Omni Directional Antennas for Use Case U1

In the corridor LOS measurements were carried out in both sections B and C. In all measurement scenarios the transmitter was located at one end of section C of the corridor as depicted in Figure VI-16.

The first set of measurement was made in section C using 10 dBi horn antennas at both transmitter and receiver. The receiver was moved along the centre line of the corridor at distances of 3, 5, 7, and 9 metres. This geometry corresponds to U14 use case, for short range backhaul where both terminals are fixed to a wall or ceiling with LOS view. These scenarios are referred to as U14-HH-3m, U14-HH-5m, U14-HH-7m, and U14-HH-9m.

Measurements were performed under identical conditions in section B of the corridor but with both terminals employing omnidirectional antennas and separated by 3 and 6 metres. These scenarios are referred to as U14-OO-3m, and U14-OO-6m as shown in Figure VI-16.

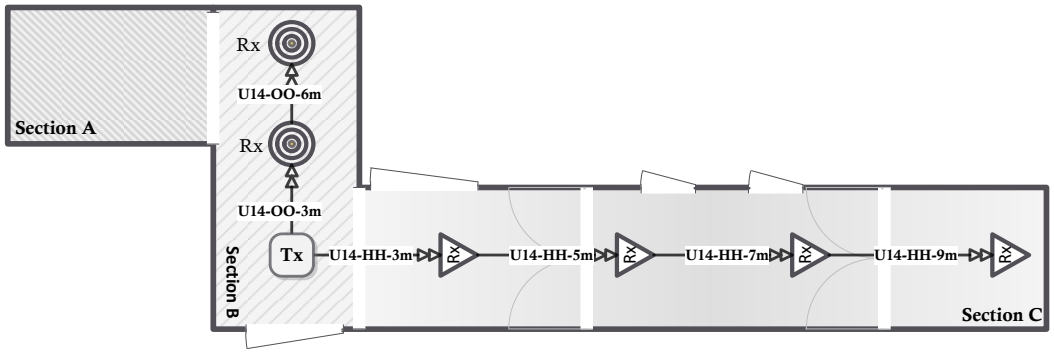


Figure VI-16 Short-Range Backhaul (U14) with Horn and Omnidirectional Transmit Antenna in a Corridor

In the corridor environment the received signal exhibits multipath fading as deep as 30 dB to 40 dB because of interference between the direct component between the transmitter and receiver and reflections off walls, ceiling and floor [65]. It is therefore expected that the received signal powers fall outside the range over which the system performance is flat. This is likely to induce additional BER values above those measured for AWGN channel.

Figure VI-17 shows results obtained in section C and B in the corridor representing U14 use case channels as illustrated in CHAPTER V. The maximum SNR penalty relative to that of the AWGN channel for a BER of 10^{-6} is around 3.8 dB.

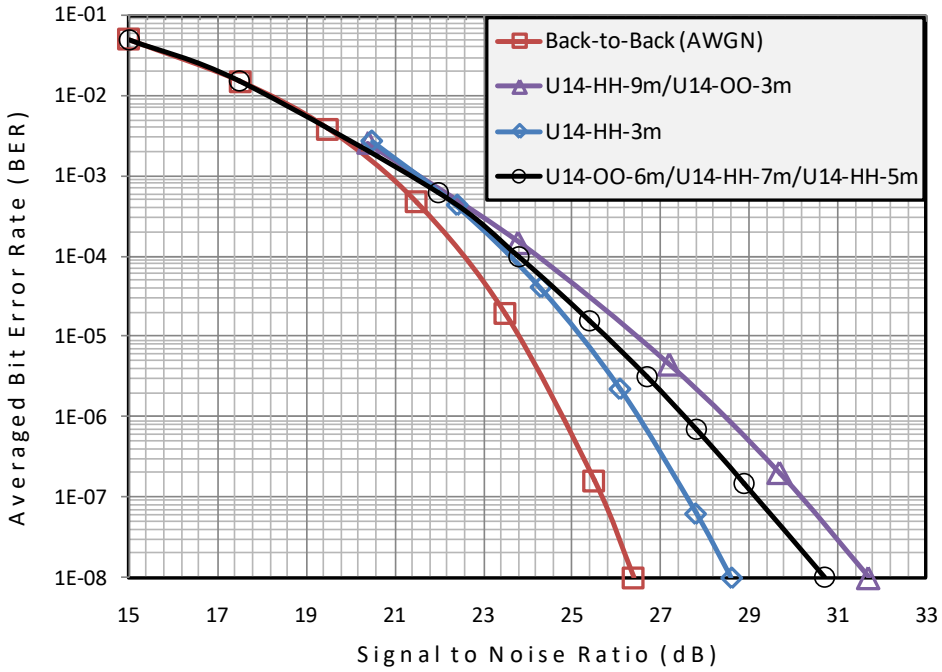


Figure VI-17 BER vs. SNR in SC-FDE for Short-Range Backhaul U14 Transmission with Horn and Omni Antennas

Considering BER performance measured under LOS and NLOS conditions utilising a combination of omnidirectional and directional transmit and receive antennas, a BER of 10^{-6} is achievable for SNRs in the range of 24.7–28.5 dB in all channels compared to 24.7 dB required in AWGN channel. Table VI.1 summarizes the SNR values required in different environments and conditions in order to achieve the maximum allowable BER of 10^{-6}.

Table VI.1 Signal-to-Noise Ratio SNR Ranges Required to Achieve 10^{-6} BER

Transmission Scenarios/Applications	SNR Range to achieve 10^{-6} BER
Desktop/Office LOS Ad-Hoc, File transfer and Sync	24.7 – 25.7 dB
Access point LOS Gigabit Ethernet, Video Streaming	25.5 – 26.4 dB
Desktop/Office NLOS Video Streaming, File Transfer, and Wireless Desktop	25.5 – 27.7 dB
Corridor LOS Short-range backhaul	26.5 – 28.5 dB

VI.6 BER Performance of the Coded SC-FDE

As described in CHAPTER IV, the SC-FDE system has been extended to include forward error control (FEC) mechanism for errors correction. The IEEE 802.15.3c standard for millimetre-wave WAPN proposes the Reed-Solomon (RS) coding scheme, with code rates equals to 1/2, 3/4 and 7/8 and code sizes of RS(200,100), RS(200,150), and RS(200,170) respectively.

The BER performance of the Coded SC-FDE, with 16-QAM modulation, has been characterized in the scenarios defined previously. Those scenarios are: U5 with LOS with horn antennas, U16 LOS with omnidirectional antennas, U8 for NLOS horn antennas, and U1 NLOS with omnidirectional antennas.

A first comparison between the theoretical and the measured BER vs. SNR in case of AWGN channel is shown in Figure VI-18, those results show the deviation from the theoretical results due to the different hardware imperfections, this deviation is about 1.5 dB in the uncoded transmission. Whereas employing coding reduces the effect of those imperfection and makes the measurement results very close to theoretical results.

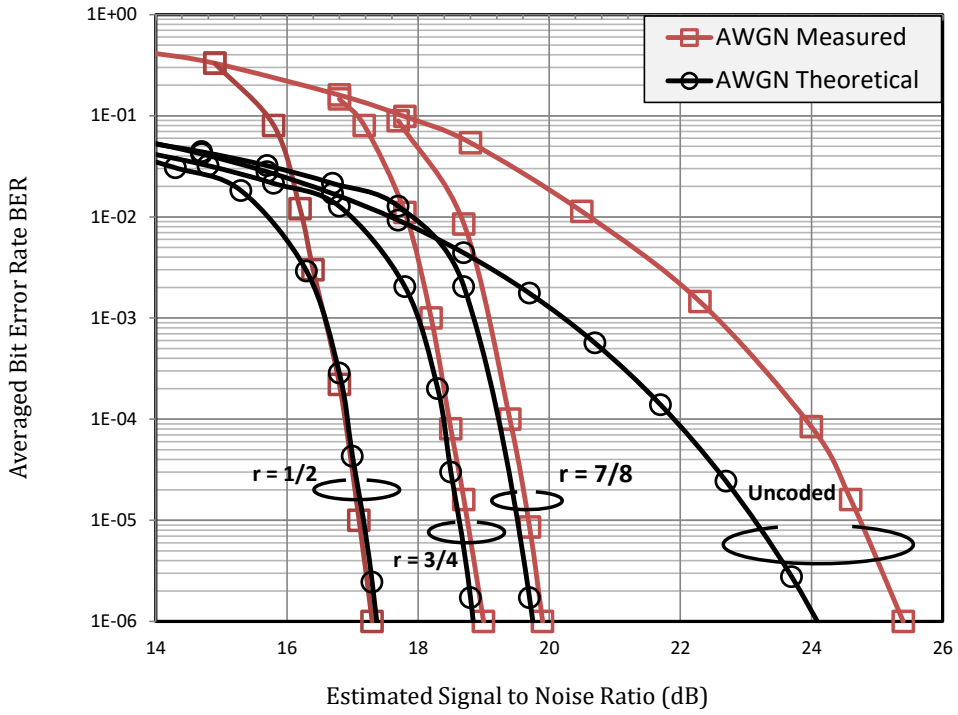


Figure VI-18 Theoretical and Measured BER vs. SNR in Coded SC-FDE Over AWGN Channel

Results recorded in the room for use case U5 where both terminals are equipped with directional antennas are given in Figure VI-19. It is clearly evident that the frequency domain equalization technique, with or without coding, is effective in mitigating the effects of multipath fading and it yields a BER performance similar to that of AWGN channel.

With the horn antennas at the transmitter and receiver replaced with omnidirectional antennas, U16 use case, the channel experiences more severe multipath propagation [65]. The SC-FDE performance obtained with and without coding is shown in Figure VI-20. Under such multipath conditions SC-FDE with RS coding is proving to be effective in reducing the effects of multipath resulting in a performance close to that obtained in AWGN channel. In such a multipath channel the degradation in the SNR for a BER of 10^{-6}, relative to AWGN channel, is around only 0.8, 0.6, and 0.5 dB for code rates of 1/2, 3/4 and 7/8 respectively. This value increases to 3.4 dB if coding is not implemented.

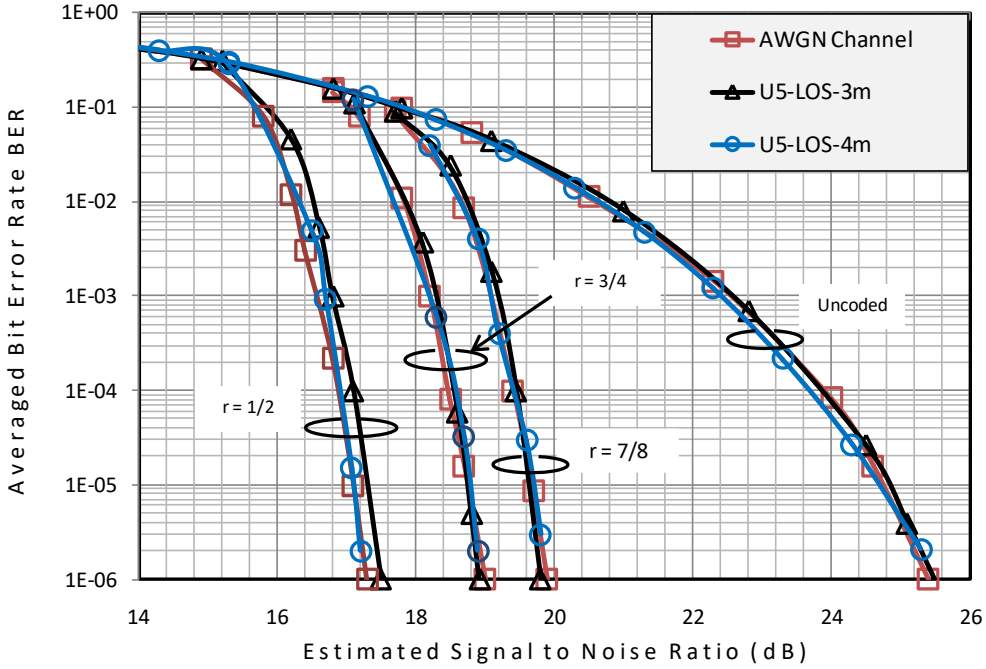


Figure VI-19 BER vs. SNR in Coded SC-FDE in U5-LOS Channels Using Directional Antennas

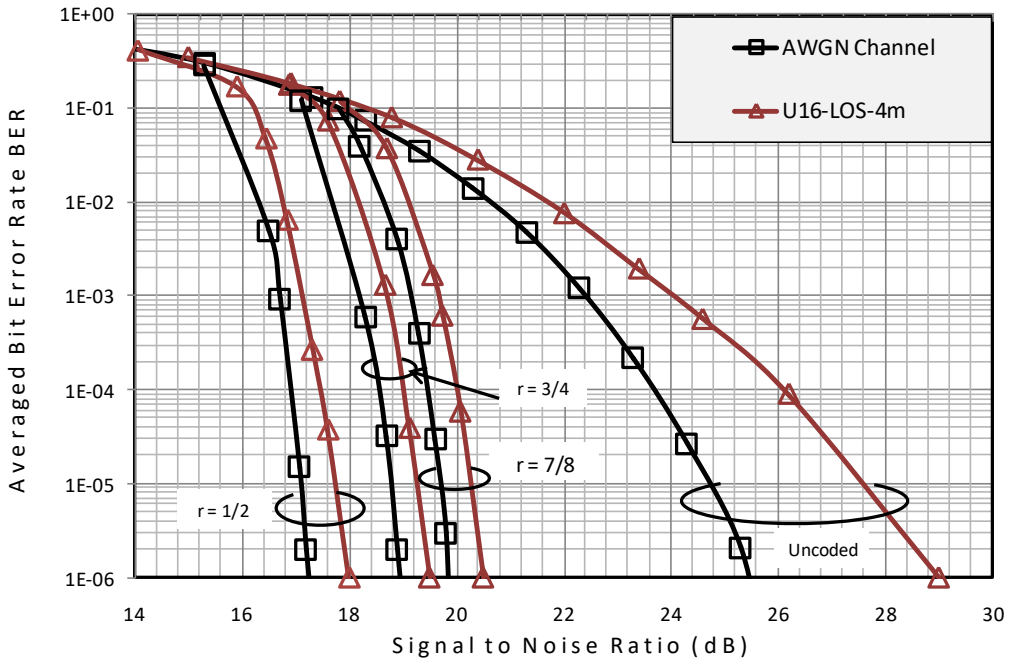


Figure VI-20 BER vs. SNR in Coded SC-FDE in U16-LOS Use Case Using Omnidirectional Antennas

For NLOS transmission, BER results measured for use case U8 are illustrated in Figure VI-21. In this scenario, where strong reflections off the wall are received, the degradation in the SNR relative to the AWGN channel is around 0.4 dB with and without coding. Whereas, in use case U1 where the received signal is highly

attenuated due the wall separating transmitter from the receiver, the SNR to achieve the 10^{-6} BER with no coding is 3.4 dB above that of the AWGN channel. This value reduces to 0.8, 1.2 and 1.6 dB by using RS coding with 1/2, 3/4 and 7/8 code rates respectively as is shown in Figure VI-22.

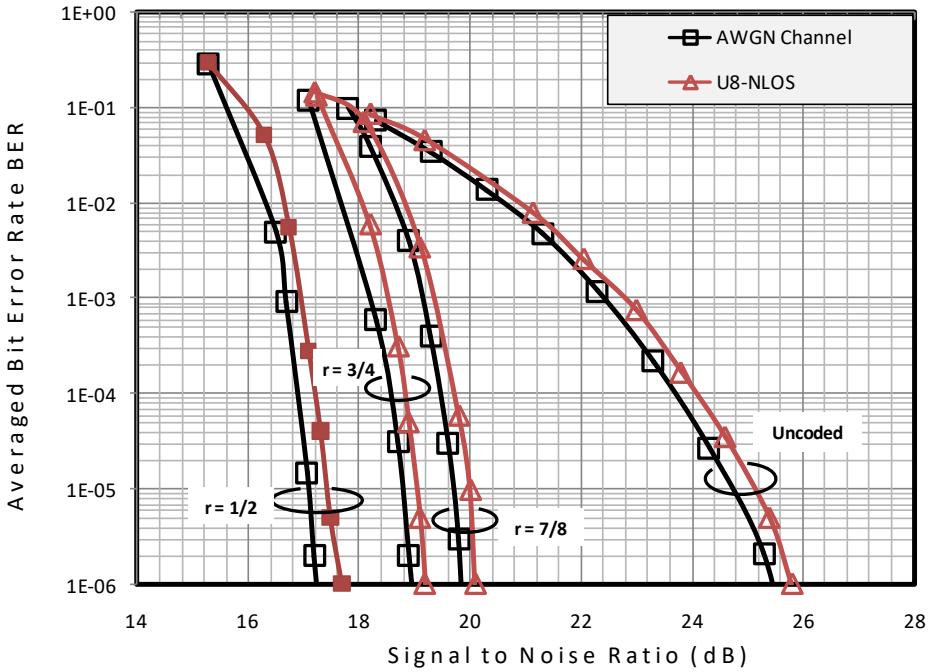


Figure VI-21 BER vs. SNR in Coded SC-FDE in U8-NLOS Use Case with Horn Transmit And Receive Antennas

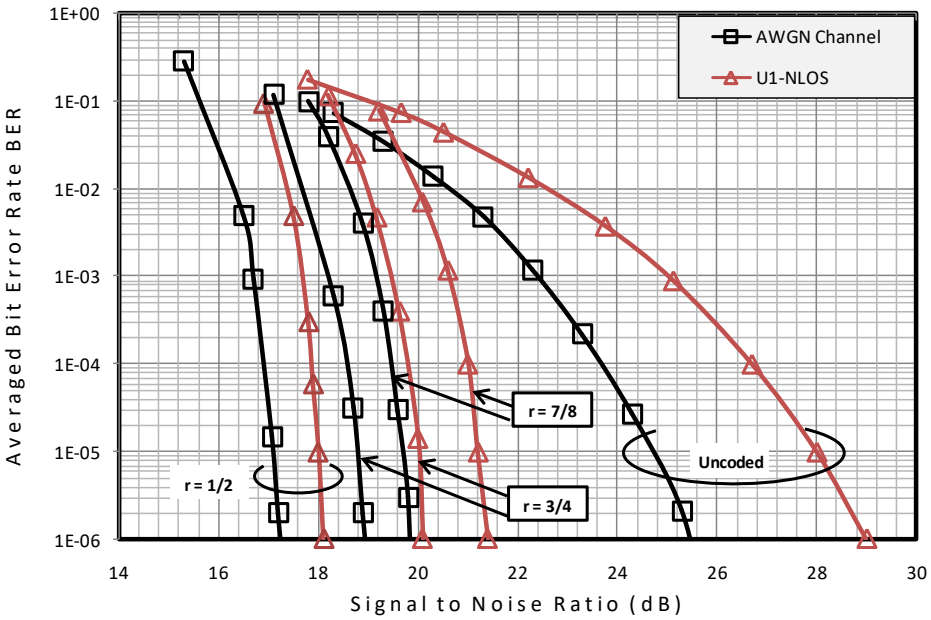


Figure VI-22 BER vs. SNR in Coded SC-FDE in U8-NLOS Use Case with Omnidirectional Antennas

Table VI.2 summarises the results obtained for the different scenarios. The frequency domain equalization technique, with no coding, has demonstrated its ability to mitigate multipath effects in indoor channels with the highest degradation in the SNR, relative to that of AWGN channel of 3.7 dB. FDE combined with RS coding yields a much improved BER performance and reduces the degradation of the SNR, relative to that of AWGN, to 0.7, 1.1, and 1.6 dB for 1/2, 3/4, and 7/8 code rates respectively.

Table VI.2 Signal-to-Noise Ratio SNR Required to Achieve 10^{-6} BER

Transmission Scenarios/Applications	SNR to achieve 10^{-6} BER			
	Uncoded	r = 1/2	r = 3/4	r = 7/8
Horn-Horn LOS Short-Range Backhaul (U5)	25.4 dB	17.4 dB	19.0 dB	19.8 dB
Omni-Omni LOS Ad-hoc, Files Transfer (U16)	29.1 dB	18.1 dB	19.5 dB	20.5 dB
Horn-Horn NLOS Files Transfer NLOS (U8)	25.8 dB	17.7 dB	19.2 dB	20.1 dB
Omni-Omni NLOS Uncompressed Video Streaming (U1)	29.0 dB	18.1 dB	20.1 dB	21.4 dB

VI.7 BER Performance of the OFDM

In this section the transmission mode is switched to OFDM scheme, the BER performance in the room of Figure VI-6, using transmit and receive horn antennas was measured with transmitter and receiver terminals are 1, 2 and 4.5 metres apart.

Figure VI-23 shows the BER vs. SNR measured in U5 use case. To maintain a maximum BER of 10^{-6} that was defined in the IEEE 802.15.3c for multimedia applications, the required SNR is 28.6 dB which equals to 2.6 dB above that of the AWGN channel when the transmitter and receiver are 1 and 2 metres apart. This SNR penalty increases to 4 dB when transmitter and receiver terminals are 4.5 metres apart. This degradation is mainly due to the fall of the received signal power, which reduces the number of effective number of bits of the ADC and gives rise to important spurious components. This effect was demonstrated when measuring the dynamic range of the receiver in OFDM transmission, given in Figure V-7, where the performance is flat only over a narrow range of input powers.

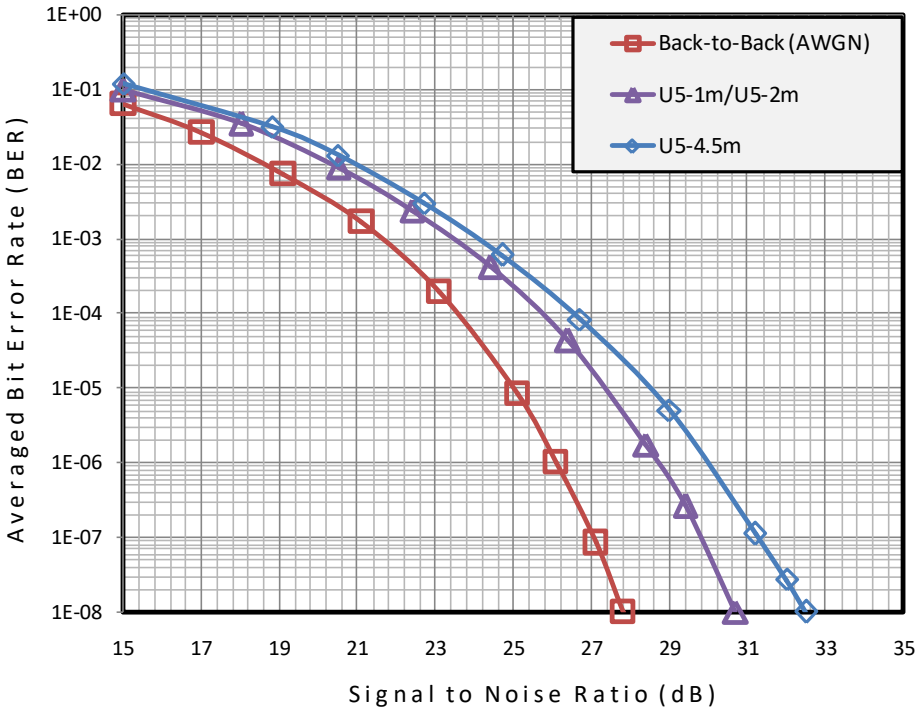


Figure VI-23 BER vs. SNR in OFDM for Line-of-Sight U5 with Horn Antennas

For use case U16, using omnidirectional transmit and receive antennas as depicted in Figure VI-8. The BER measurement of Figure VI-24 shows a further degradation compared to the previous measurements performed with horn antennas. This due to the fact that employing omnidirectional antennas the channel will experience more severe multipath propagation and yields to a further degradation of the received signal power. The SNR required to achieve a BER of 10^{-6} is 2.6 and 4.8 dB greater than that needed in AWGN channel when transmitter and receiver are 2 and 4.5 metres apart respectively.

In use case U17 with a horn receive antenna, the BER performance shown in Figure VI-25 shows an increase of SNR penalties to achieve the required BER of 10^{-6}. In this case a SNR of 4 and 7 db above that of AWGN channel is required. Furthermore, the OFDM system fails to achieve the 10^{-6} BER when transmitter and receiver are 3 metres apart.

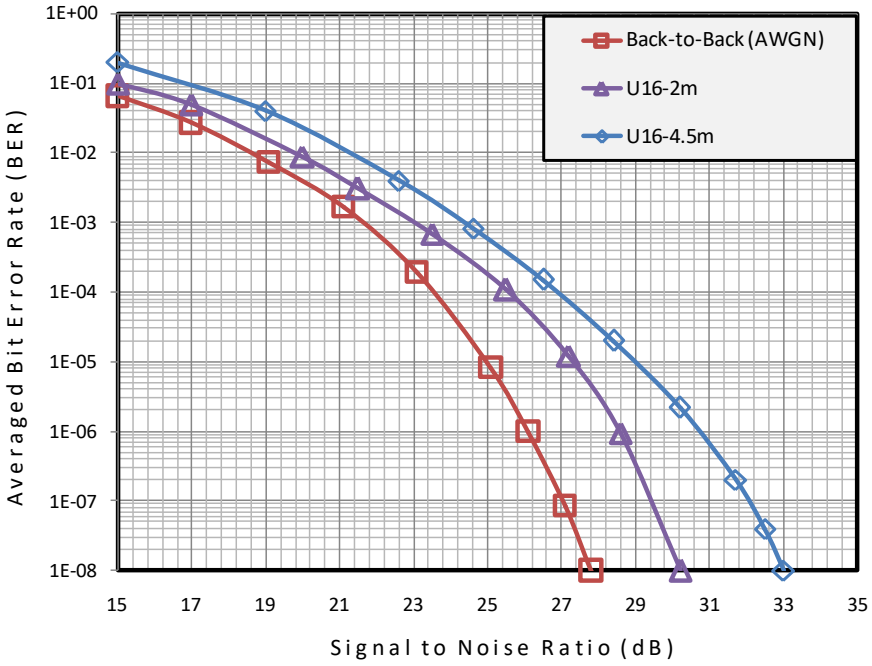


Figure VI-24 BER vs. SNR in OFDM for LOS U16 Transmission with Omnidirectional Antennas

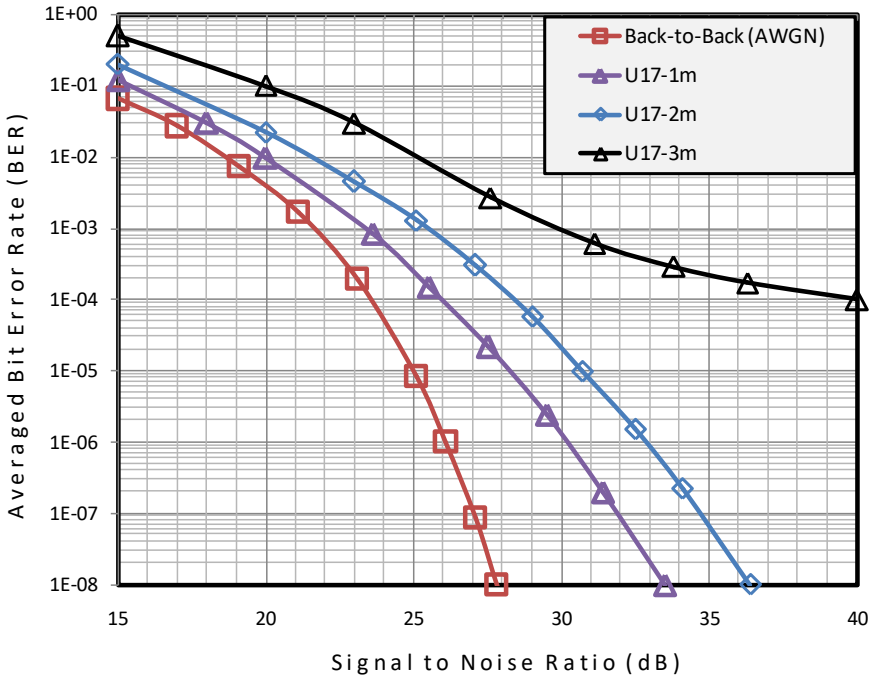


Figure VI-25 BER vs. SNR in OFDM for LOS U17 Transmission with Omnidirectional Transmit and Horn Receive Antenna

In NLOS transmissions (U8 and U1 use cases), and LOS in corridor for backhaul link (U14), the OFDM modulation scheme fails to achieve the required 10^{-6} BER, and an infinite degradation occurs. Therefore, no BER measurements have been done in such scenarios.

The overall BER vs. SNR performance of the SC-FDE and OFDM communication schemes over the AWGN and indoor channels is shown in Figure VI-26. The SC-FDE shows consistent results compared to that of OFDM modulation scheme, in which performance degradation spreads over a large surface. This makes the OFDM not reliable to work in such RF frontend, unless impairments associated with the 64.8 GHz frontend (i.e., PA nonlinearity, phase noise, IQ-imbalances etc.) are compensated.

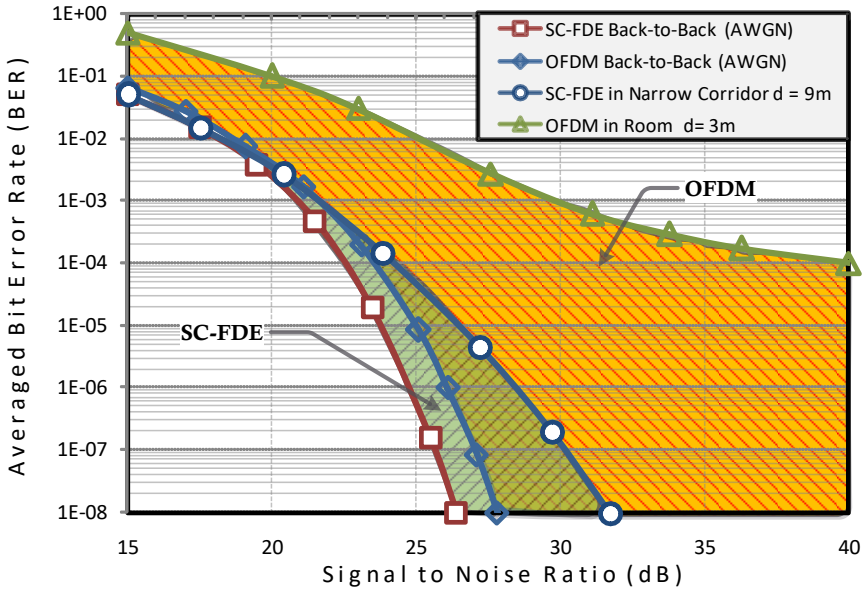


Figure VI-26 Overall BER vs. SNR Performance in SC-FDE and OFDM Communication Schemes

VI.8 Uncompressed Video Transmission

Real time transmission of an uncompressed video through the 64.8 GHz system given in Figure V-2 has been achieved and demonstrated using Matlab Simulink as graphical user interface. Figure VI-27 shows the transmitted and the received video along with the 16-QAM received constellation and the respective SNR value. The transmitter and receiver were 4 metres apart with omnidirectional antennas at both terminals. The quality of the received video matches to that of the transmitted one, and no differences can be discerned.

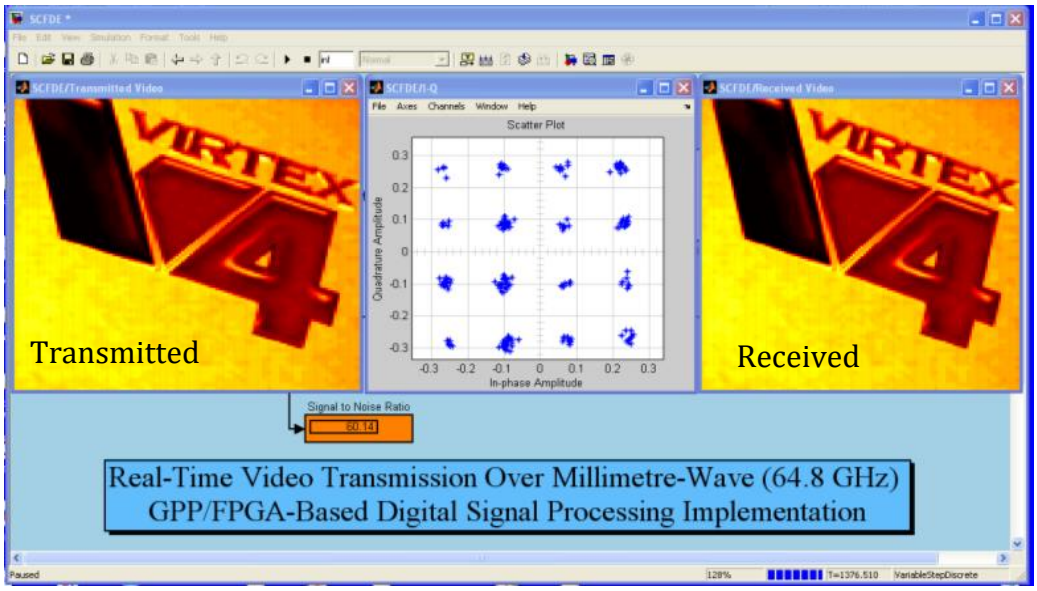


Figure VI-27 Real-Time Video Transmission at 64.8 GHz

VI.9 Conclusion

In this chapter, the effectiveness of the SC-FDE and OFDM communication techniques with 16-QAM modulation and FDE equalization, to cope with both effects of multipath propagation and the impairments associated with the 64.8 GHz RF frontend has been demonstrated, by measuring the BER against SNR in a number of indoor channels under LOS and NLOS conditions.

To characterize the real BER performance of the implemented 64.8 GHz transceiver with SC-FDE and OFDM communication scheme, different transmission scenarios have been identified. Those scenarios reflect a number of propagation patterns within diverse geometries that may generate different multipath severities and received signal powers. Either the transceiver's terminals are mobile (e.g., ad-hoc application) or fixed (e.g., backhaul link), BER performance characterization was carried out in a room and corridor respectively.

The higher robustness of the SC-FDE compared to OFDM was clearly made in evidence. For LOS transmission in a room environment (e.g., office, desktop) the SNR required to achieve a similar performance to that of the AWGN channel is not more than 0.6 dB and 1 dB for horn and omnidirectional antennas respectively for a BER of 10^{-6}, whereas, in OFDM the SNR penalty reaches 4 dB in similar conditions.

Furthermore, under NLOS conditions and in a long corridor, the SC-FDE keeps operating within acceptable performance where the SNR penalty is about 3 dB and

3.8 dB above that of AWGN channel in the room with NLOS and corridor respectively. However, the OFDM totally fails to achieve an acceptable BER performance under those conditions.

The higher performance of the SC-FDE obtained in different scenarios, have encouraged us to further extend it and include forward error control (FEC) in order to correct the residual bit-errors. Results have shown that the SNR penalty, relative to that of AWGN channel, decreases with the use of FDE combined with RS coding. For all measurement scenarios the SNR measured for a BER of 10^{-6} using SC-FDE varies between 25.4 dB and 29 dB giving a 3.6 dB variation. This variation reduces to 0.7, 1.1 and 1.6 dB when SC-FDE is combined with RS coding for 1/2, 3/4 and 7/8 code rates respectively.

CHAPTER VII
Conclusions and Future Work

VII.1 Introduction

In this thesis we have successfully demonstrated the novelty of designing and implementing a millimetre-wave wireless communication link, operating at the 64.8 GHz frequency. The design is based on the new IEEE 802.15.3c standard for 60 GHz frequency band, employing both single-carrier with frequency domain equalization (SC-FDE) and orthogonal frequency-division multiplexing (OFDM) communication schemes and targets a data rate up to 5 Gb/s for short range indoor applications.

The performance of SC-FDE and OFDM communication schemes has been characterized. The bit-error rate (BER) against signal-to-noise ratio (SNR) has been measured in a room and corridor, which present typical indoor channels of a 60 GHz wireless personal area network (WPAN), under line-of-sight (LOS) and non-line-of-sight (NLOS) conditions to closely represent various use case scenarios.

This chapter summarises the results obtained along with conclusions drawn from the performance of the implemented the 64.8 GHz wireless communication system. This will lead to define the direction and recommendations of the future work.

VII.2 Discussions and Conclusions

1. The first conclusion is related to the baseband implementation point of view of both SC-FDE and OFDM systems. The two implementations consume a similar amount of FPGA's resources, also they share the same functional blocks, which make the two implementations having a similar complexity and can coexist on the same platform.

2. Performance evaluation made over the emulated multipath channels, where the imperfections of the RF frontend are ignored. Have shown that both SC-FDE and OFDM have a comparable ability to mitigate the multipath effects over channels with line-of-sight (LOS) and non-line-of-sight (NLOS) conditions with severe multipath dispersion.

3. When comparing the two transmission modes over the emulated AWGN and multipath channels, the SC-FDE has shown a better performance than OFDM. This was mainly due to the complexity of the OFDM signal, which consists of much higher number of amplitude's levels compared to a single-carrier signal which consists of only four levels in 16-QAM modulation. This makes the OFDM signal very sensitive to the effect of the limited number of bits in the ADC converter that leads to strong spurious components and quantization noise.

4. Interfacing the baseband module with the 64.8 GHz millimetre-wave frontend, where the inherent imperfections (e.g., PA nonlinearity, phase-noise, IQ imbalances, etc.) of the RF frontend cause the transmitted signal to be distorted. In this case the SC-FDE showed a great robustness against those imperfections with minor degradation occurs. Whereas, the OFDM has shown great weakness against them and intolerable degradation happens, especially when a high power is being transmitted. This mainly due to the high peak-to-average power ratio (PAPR) of an OFDM signal, which limits the back-off region of the power amplifier (PA) employed at the transmitter.

5. The constructed 64.8 GHz wireless system has been deployed for real transmissions in indoor channels, with different terminals separations and varying multipath severities with LOS and NLOS conditions. In the OFDM scheme, the effects of the RF frontend imperfections adversely affect the performance of the OFDM, which limits the dynamic range of the OFDM receiver. Therefore, the OFDM system is able to operate only within limited terminals separations (between 2 and 4 metres). At larger distances, the OFDM system becomes unable to deliver a reliable wireless link and the BER vs. SNR disperse over a huge region (as shown in Figure VI-26), making the performance of the implemented OFDM system unpredictable.

6. In contrast to the OFDM, the SC-FDE transmission technique has demonstrated a great robustness in mitigating both the multipath effects of the indoor channels and imperfections associated with the RF frontend. This has been shown in the consistency of the BER vs. SNR results obtained for different transmission scenarios and separations between terminals discussed in CHAPTER VI. The overall results of the BER vs. SNR shown in Figure VI-26 are clear evidence of the advantage of the SC-FDE over the OFDM when operating with a frontend with imperfections, particularly

the nonlinearity of the power amplifier. The maximum SNR penalty to achieve the 10^{-6} BER was 3.8 dB in the corridor (for backhaul link) with a maximum distance of 9 metres, as shown in Figure VI-17. This case presents the worst case scenario in term of the received signal level and multipath severity, where the SC-FDE was able to cope with it and keeps showing an acceptable performance.

7. The extension of the SC-FDE to include forward error control (FEC) mechanism and recover the residual errors has further improved the performance of the SC-FDE. The employed Reed Solomon (RS) coding scheme with 1/2, 3/4, and 7/8 code rates has enhanced the robustness of the SC-FDE. The SNR penalty to achieve 10^{-6} BER relative to that of an AWGN channel has been reduced to 0.7, 1.1 and 1.6 dB for 1/2, 3/4, and 7/8 code rates respectively, instead of 3.7 dB SNR penalty with the uncoded SC-FDE.

8. As a case study, the IEEE 802.15.3c standard for wireless communications in the 60 GHz frequency band, and due to the limitations of the current technology in terms of designing devices with high linearity and low distortions. The SC-FDE has been selected as one of the prominent alternative to OFDM for IEEE 802.15.3c because it benefits from several interesting properties as previously described. Whereas, the OFDM is currently reserved for high cost, high data rate (up to 5 Gb/s) applications; otherwise for future advances in the very high frequency RF chips.

9. Finally, the high performance shown by the SC-FDE allowed the realization of a real time video transmission. Where for demonstration purpose, uncompressed video has been transmitted with high fidelity over a distance of 4 metres with omnidirectional antennas at both transmitter and receiver.

VII.3 Future Work

On the basis of the obtained results, and for the continuation of the study presented in this thesis, there is still much work to do, particularly in the OFDM system. Thus, the points to be considered for any further development of the implemented millimetre-wave wireless communication system:

1. The OFDM system requires further improvements to mitigate the nonlinearity of the transmitter power amplifier. This could be achieved by reducing the peak to average power ratio (PAPR) of the transmitted OFDM signal by using different

approaches, or implementing post/pre-distortion mechanisms to compensate the nonlinearity of the power amplifiers.

2. An extension of both SC-FDE and OFDM communication schemes to mitigate the impairments of the inherent RF frontend imperfections, these include: IQ imbalance, phase noise and DC-offset. An FPGA implementation of algorithms to perform estimation and compensation of those imperfections leads to improve the BER performance, especially to improve the low performance shown by the OFDM system.

3. Due the fact that the degradation of the performance in either SC-FDE or OFDM communication scheme is mainly due the decrease of the received signal power, which makes the ADC operates at very low performance. Hence, an analogue automatic gain control (AGC) should be implemented before the ADC converter, this AGC may be implemented at the RF or IF frontends to keep the analogue IQ signals within the dynamic range of the baseband receiver.

List of Publications

International Conference Papers:

K. Sobaihi, A. Hammoudeh, and D. Scammell, "**FPGA Implementation of OFDM Transceiver for a 60GHz Wireless Mobile Radio System**," in *Reconfigurable Computing and FPGAs (ReConFig), 2010 International Conference on*, 2010, pp. 185-189.

K. Sobaihi, A. Hammoudeh, and D. Scammell, **"FPGA implementation of Frequency Domain Equalizer with time domain channel estimation for millimetre-wave OFDM system,"** in *Wireless Telecommunications Symposium (WTS), 2012*, 2012, pp. 1-6.

K. Sobaihi, A. Hammoudeh, and D. Scammell, "**Automatic Gain Control on FPGA for Software-Defined Radios**," in *Wireless Telecommunications Symposium (WTS), 2012*, 2012, pp. 1-4.

K. Sobaihi, A. Hammoudeh, and D. Scammell, "**FPGA Implementation of SC-FDE for 60 GHz WPAN**" IEEE International Symposium on Personal, Indoor and Mobile Radio Communications, 2012.

Papers presented at University of Glamorgan Student Workshop:

K. Sobaihi, A. Hammoudeh, and D. Scammell, **"Carrier Recovery and Automatic Gain Control on FPGA's based platform (IEEE 802.15.3c mm-Wave PHY Application)",** *Proceeding of the 6th Research Student Workshop, Faculty of Advanced Technology, University of Glamorgan, UK, March 2011.*

K. Sobaihi, A. Hammoudeh, and D. Scammell, **"FPGA Implementation of OFDM Transceiver for a 60GHz Wireless Mobile Radio System",** *Proceeding of the 5th Research Student Workshop, Faculty of Advanced Technology, University of Glamorgan, UK, March 2010.*

Journal Papers:

K. Sobaihi, A. Hammoudeh, and D. Scammell, **" Design and FPGA Implementation of Frames Detector for SC-FDE/OFDM Millimetre Wave IEEE802.15.3c WPAN,"** Cyber Journals: Journal of Selected Areas in Telecommunications (JSAT), July Edition, 2012.

K. Sobaihi, A. Hammoudeh, and D. Scammell, **"FPGA-Based Software-Defined Radio for Millimetre-Wave Single-Carrier Transmission"**, Accepted for publication by IET Journal on Networks.

Appendix A
System Generator Implementation of SC-FDE and OFDM Baseband Main Modules

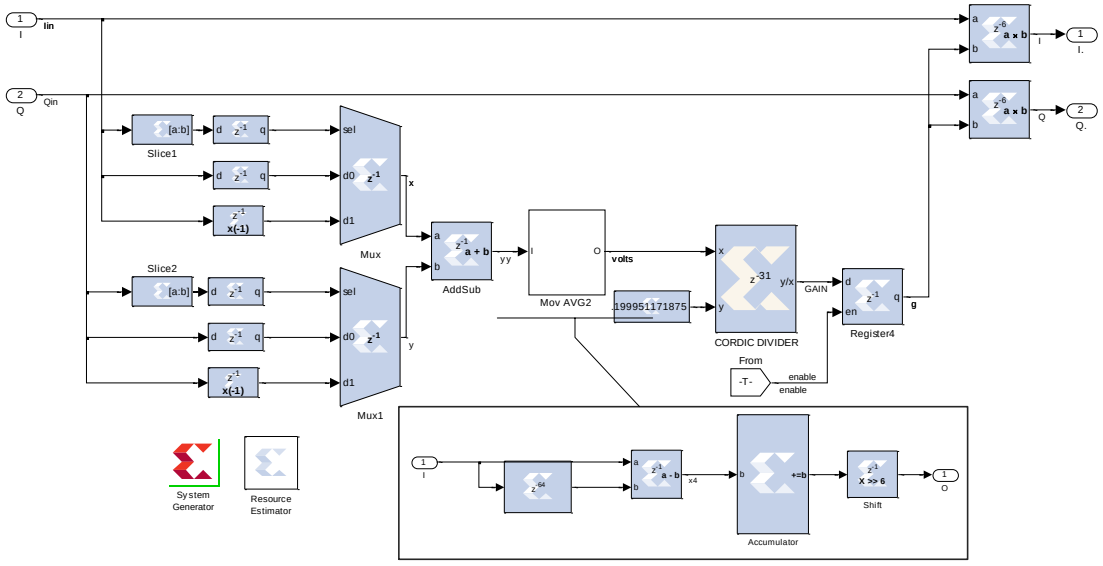


Figure A.1 System Generator Implementation of Feed-Forward AGC

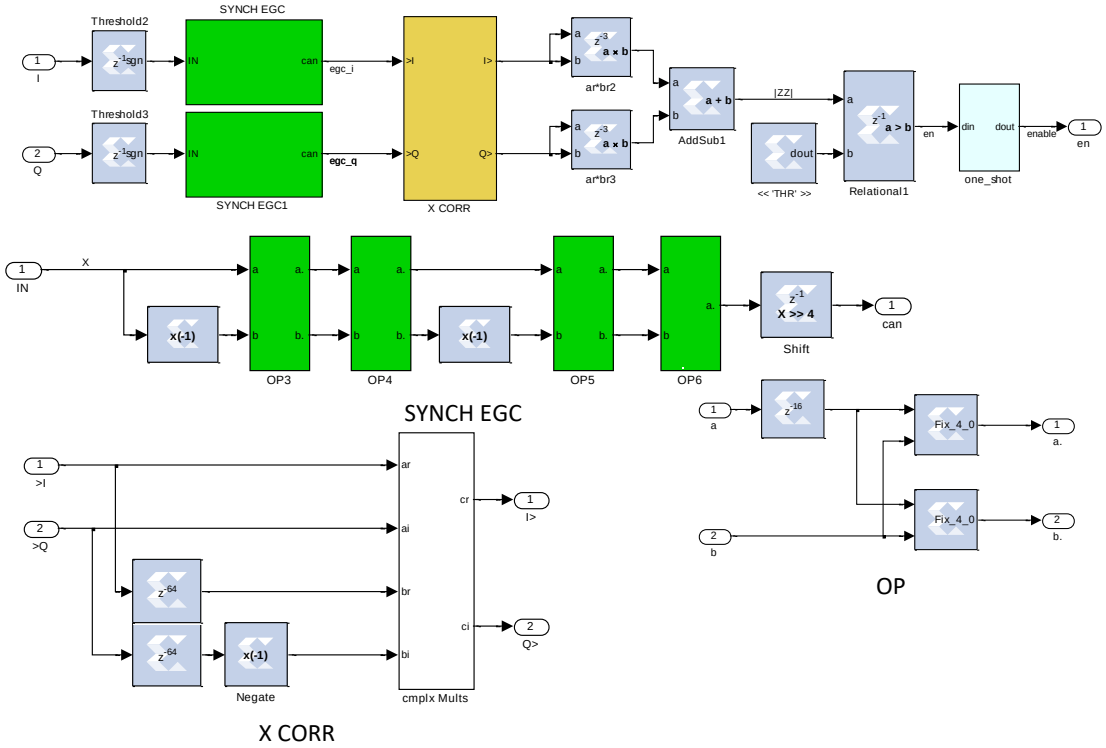


Figure A.2 System Generator Implementation of Start Frame SFD Detector

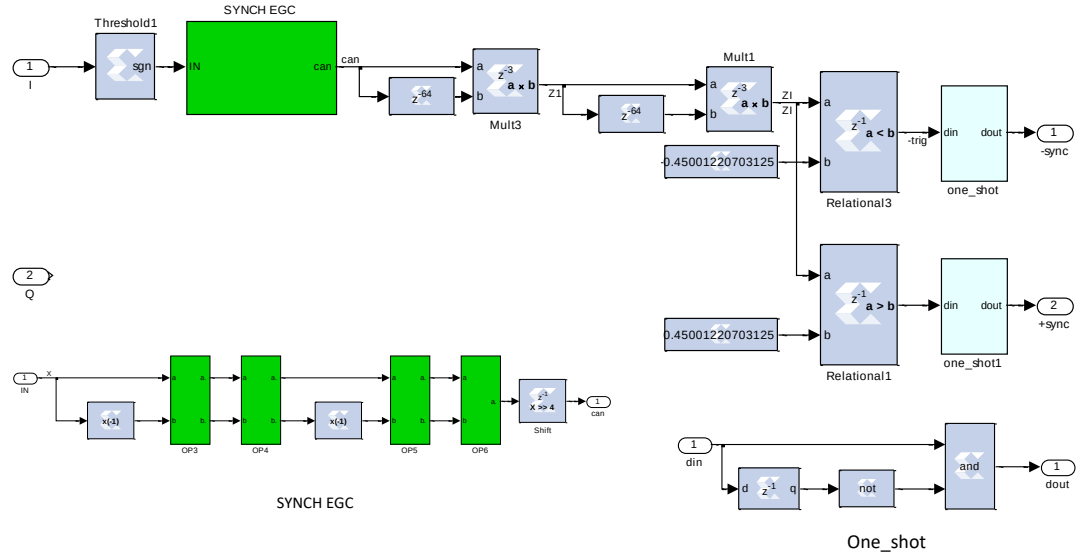


Figure A.3 System Generator Implementation of SYNC Frame Detector

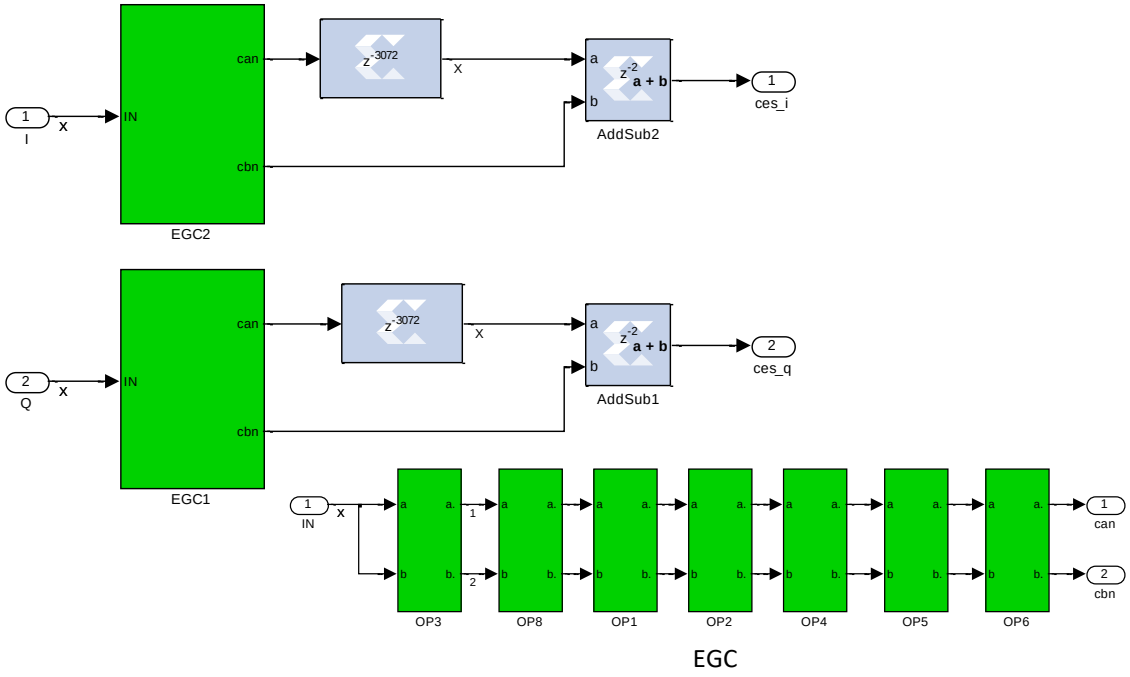


Figure A.4 System Generator Implementation of Channel Impulse Response Estimator

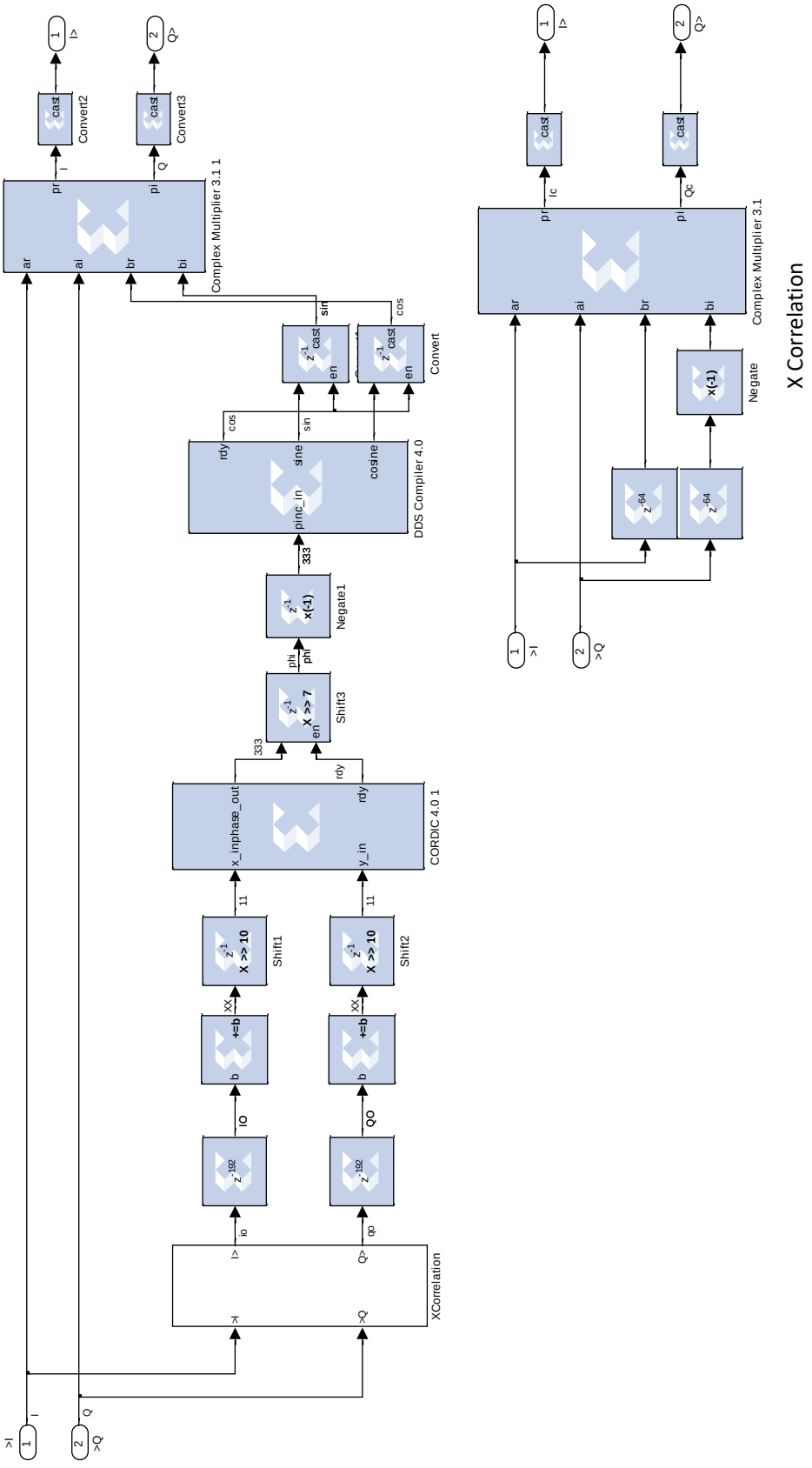
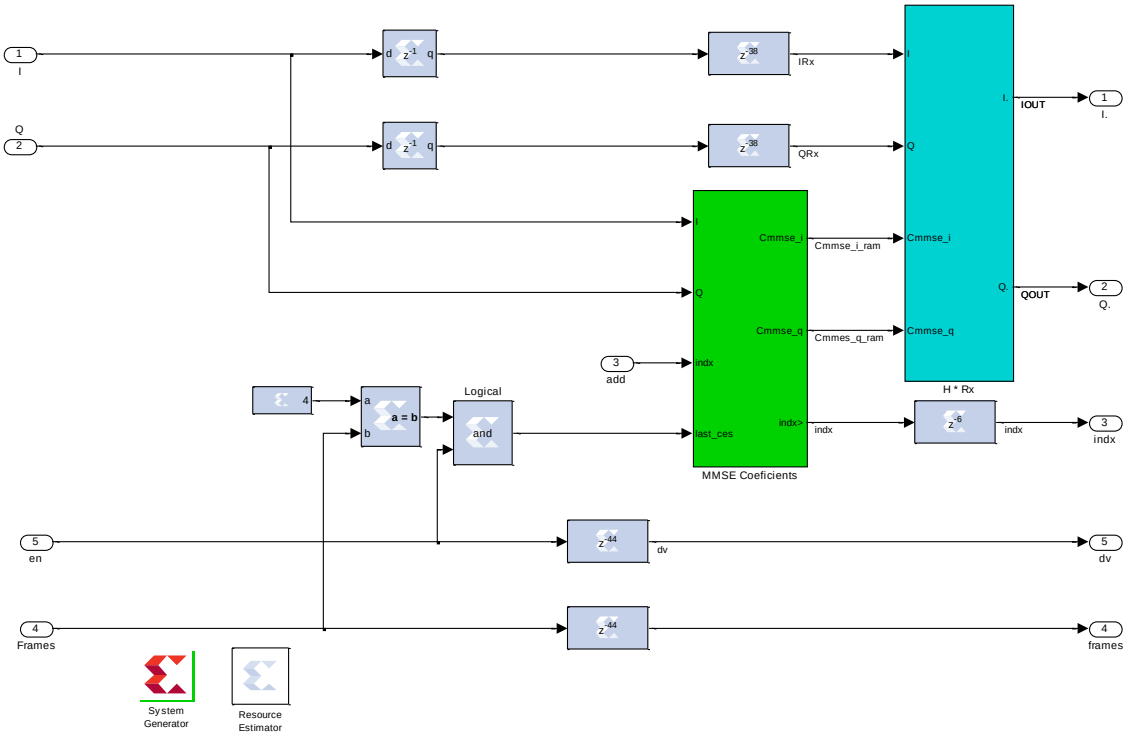
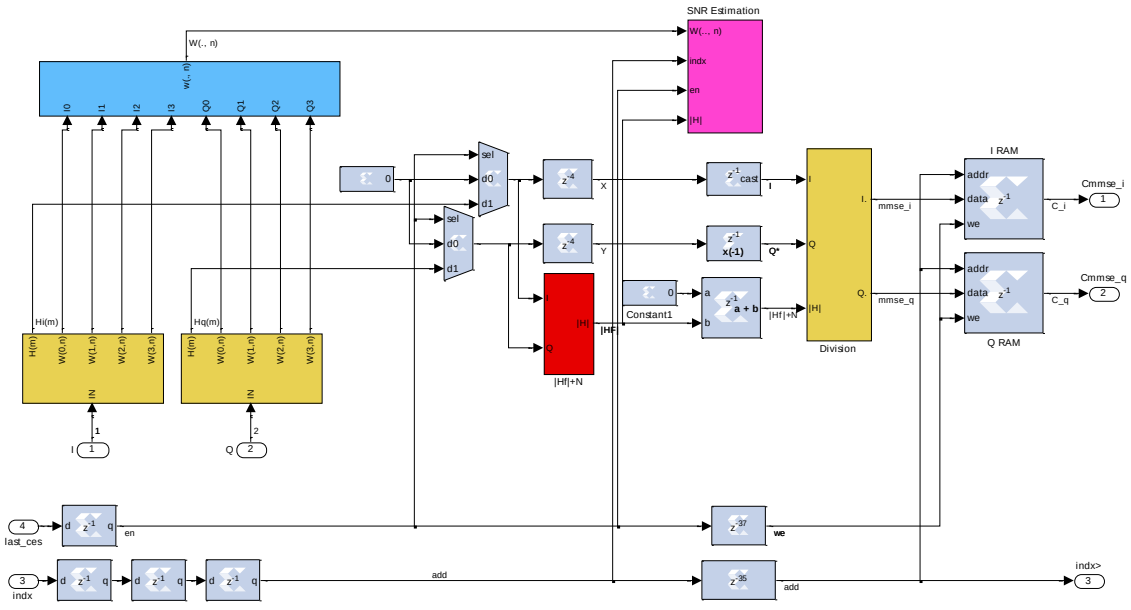


Figure A.5 System Generator Implementation of Carrier Recovery



Frequency Domain Equalizer



MMSE Coefficients Calculator

Figure A.6 System Generator Implementation of Frequency Domain Equalizer

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